OBFUSCURO: A Commodity Obfuscation Engine for Intel SGX

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(* denotes equal contribution)

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Program Obfuscation

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Trusted

Untrusted (except the Black box)

Sender's Goal
Protect the internals of private program P_{priv}

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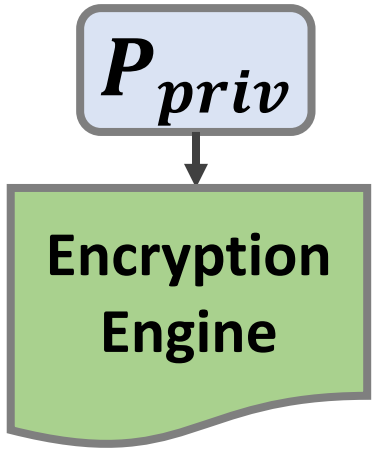

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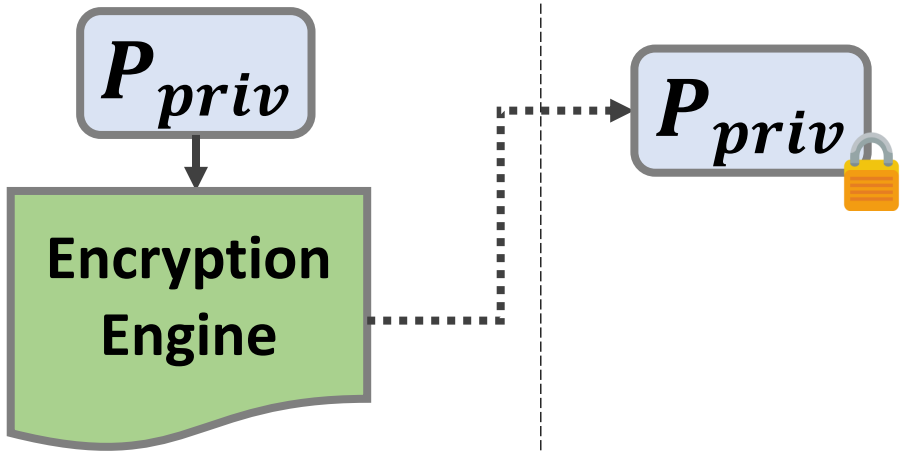

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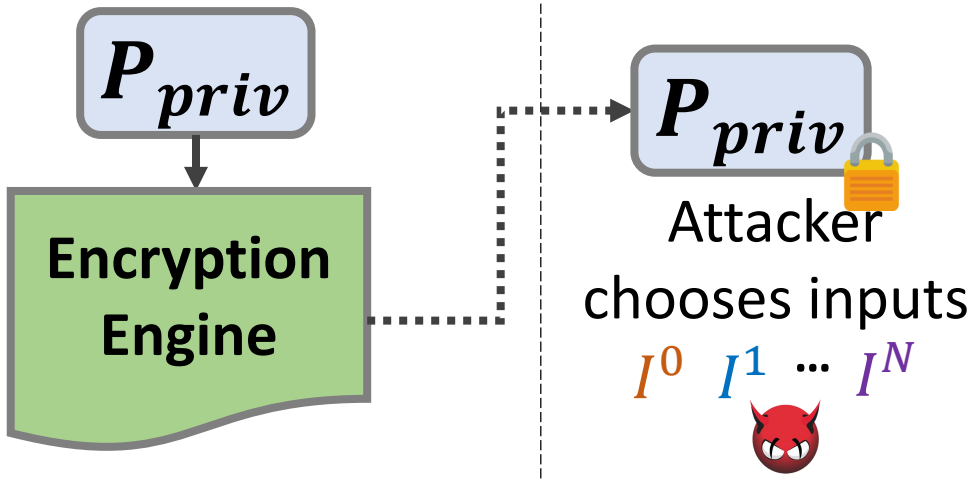

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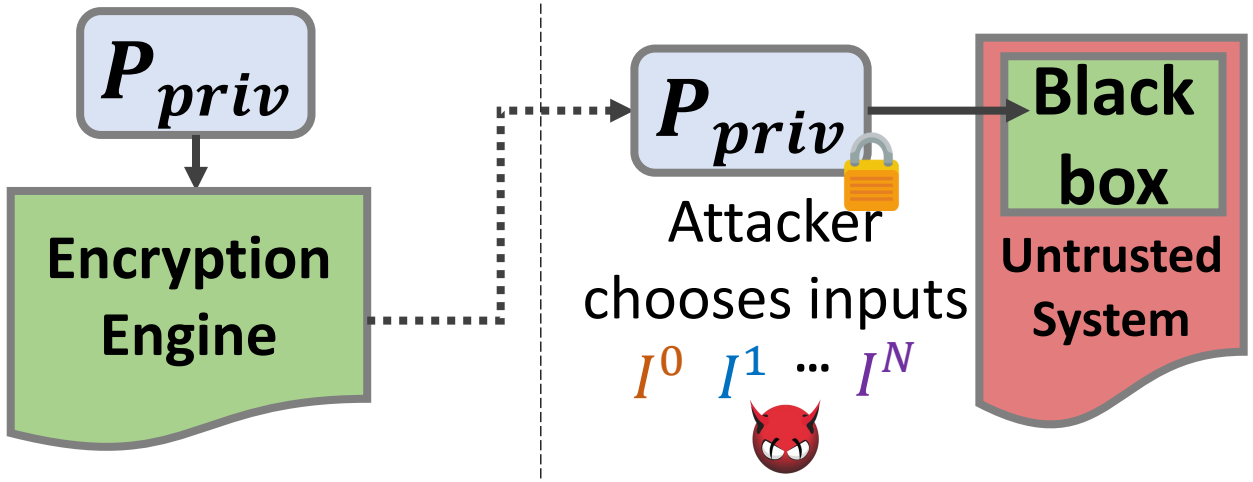

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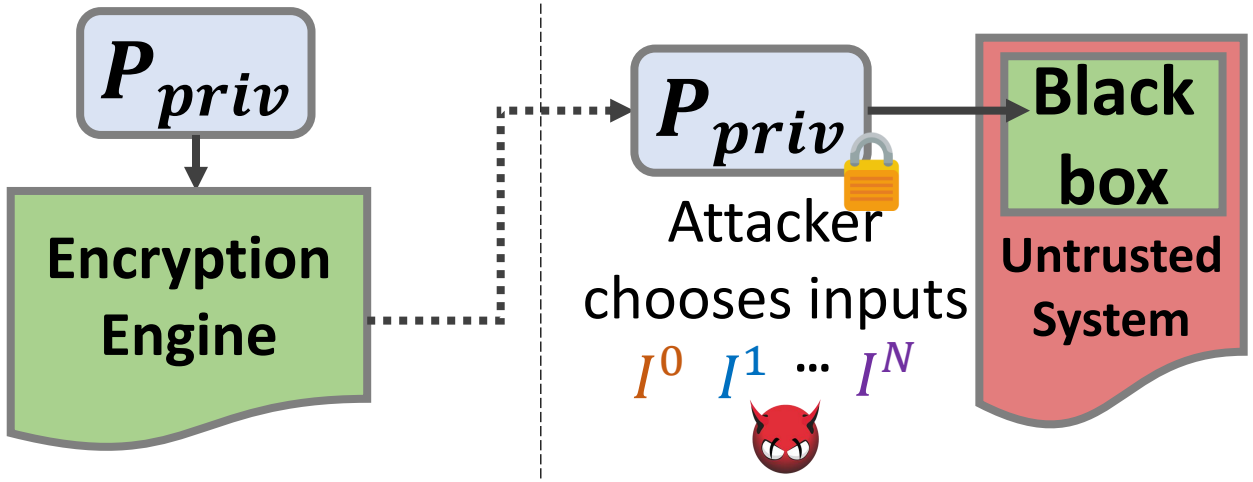

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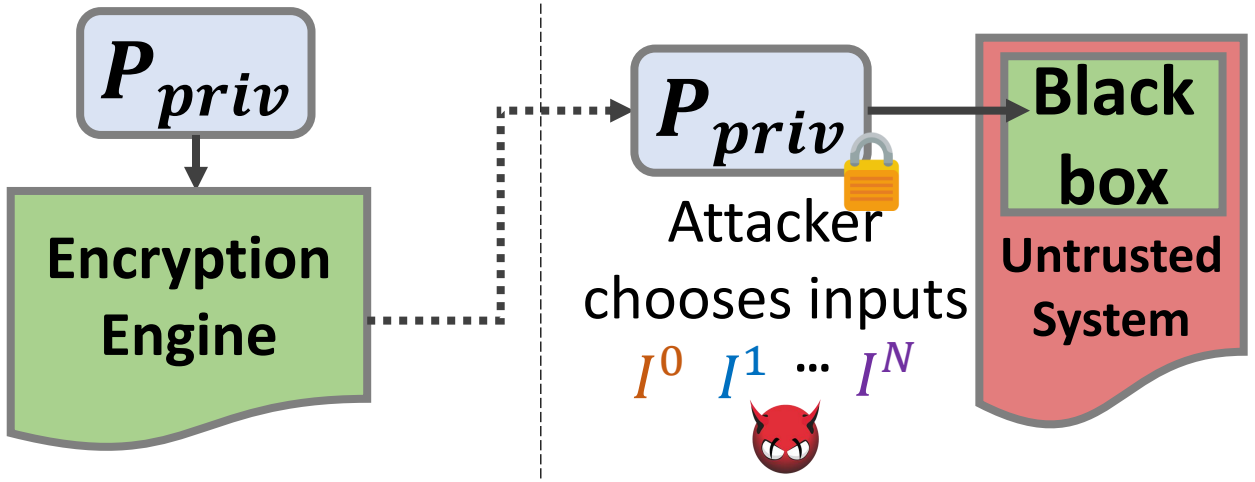
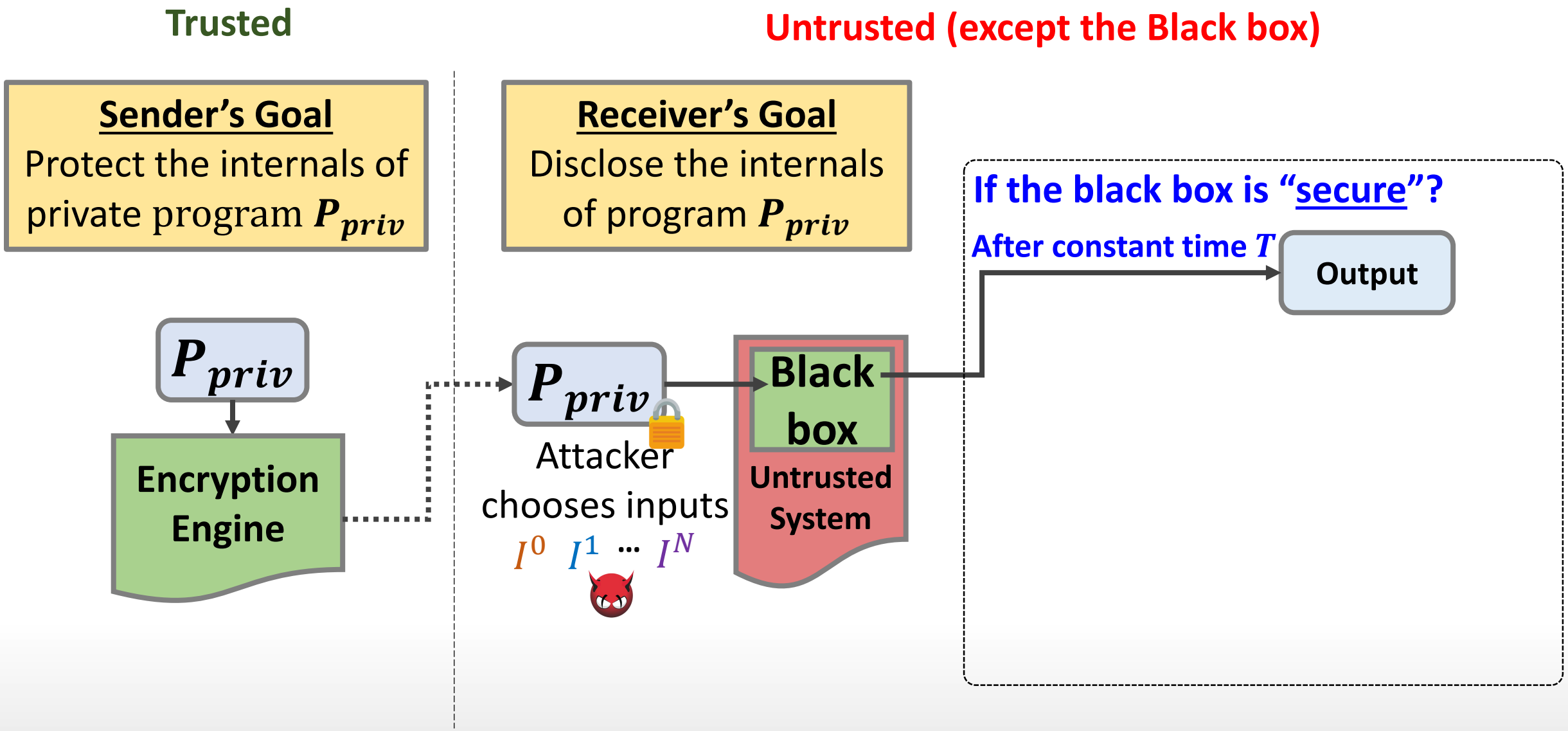


If the black box is "secure"?

Program Obfuscation



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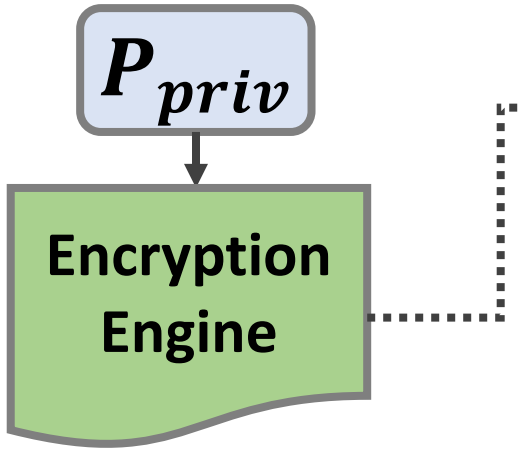

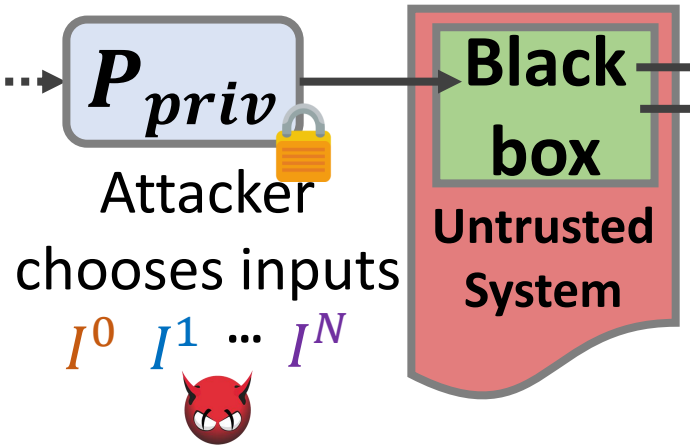

If the black box is "secure"?

After constant time T → **Output**

Observable execution traces
Φ^0 Φ^1 … Φ^N

Execution traces ***should not leak*** information about P_{priv}

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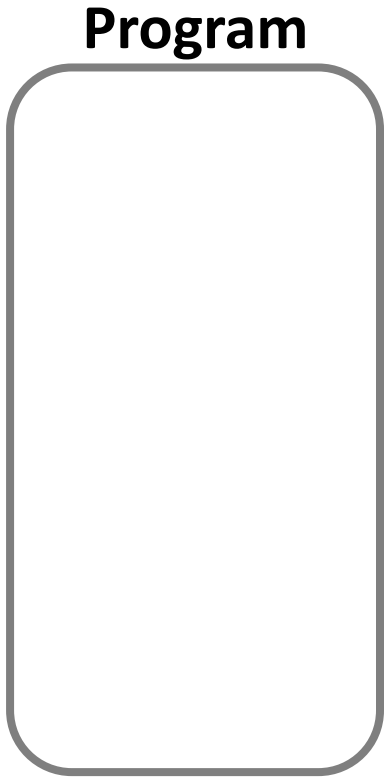

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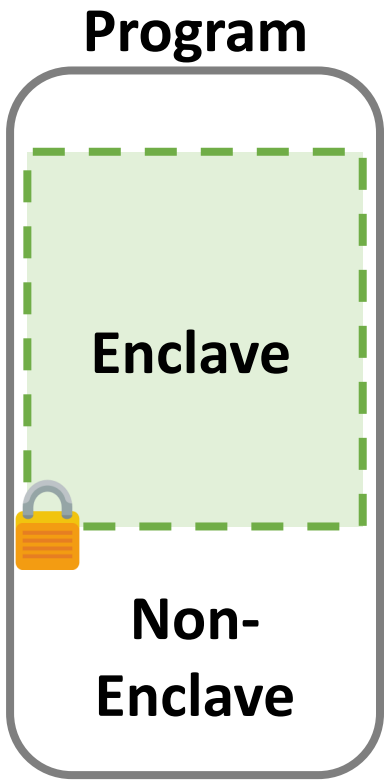

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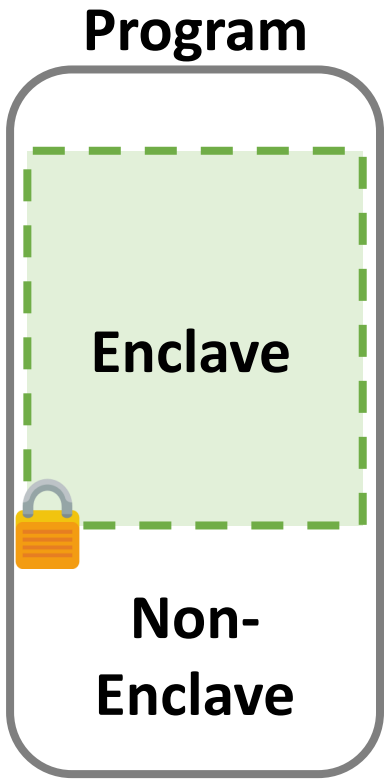
Trusted execution region

Confidentiality and ***integrity*** guarantees



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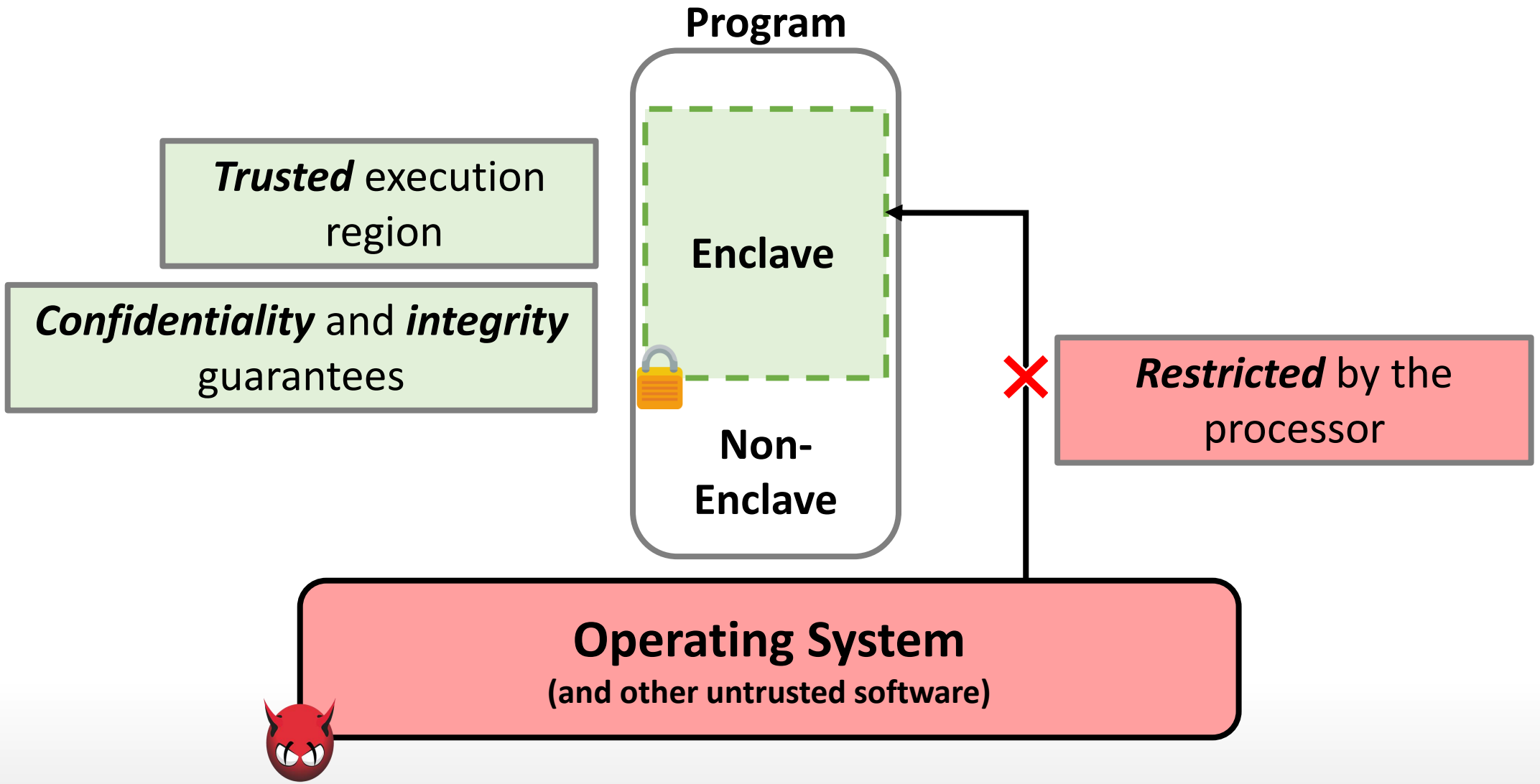

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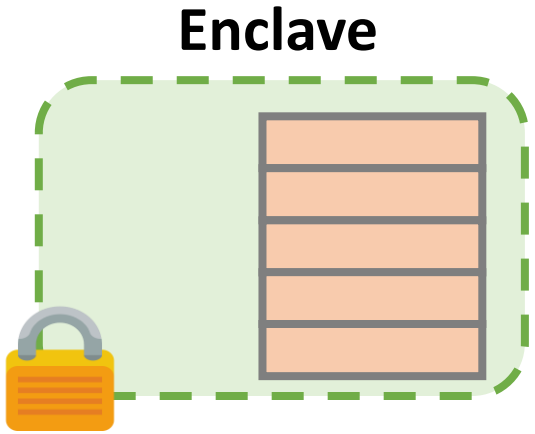

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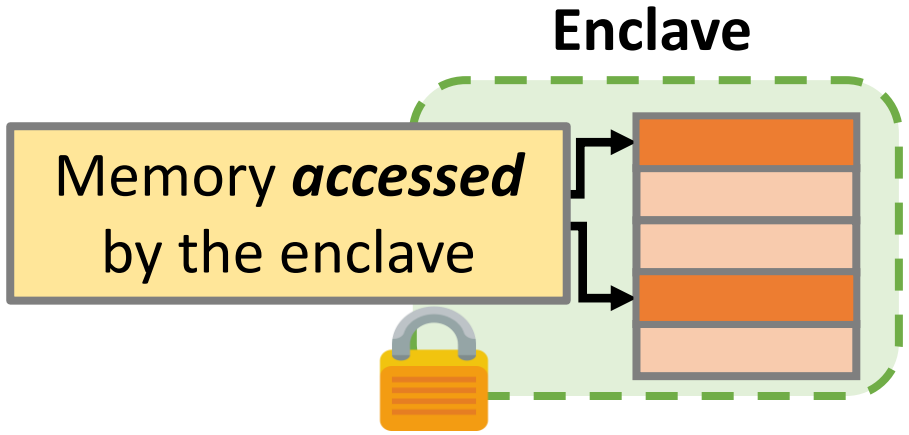

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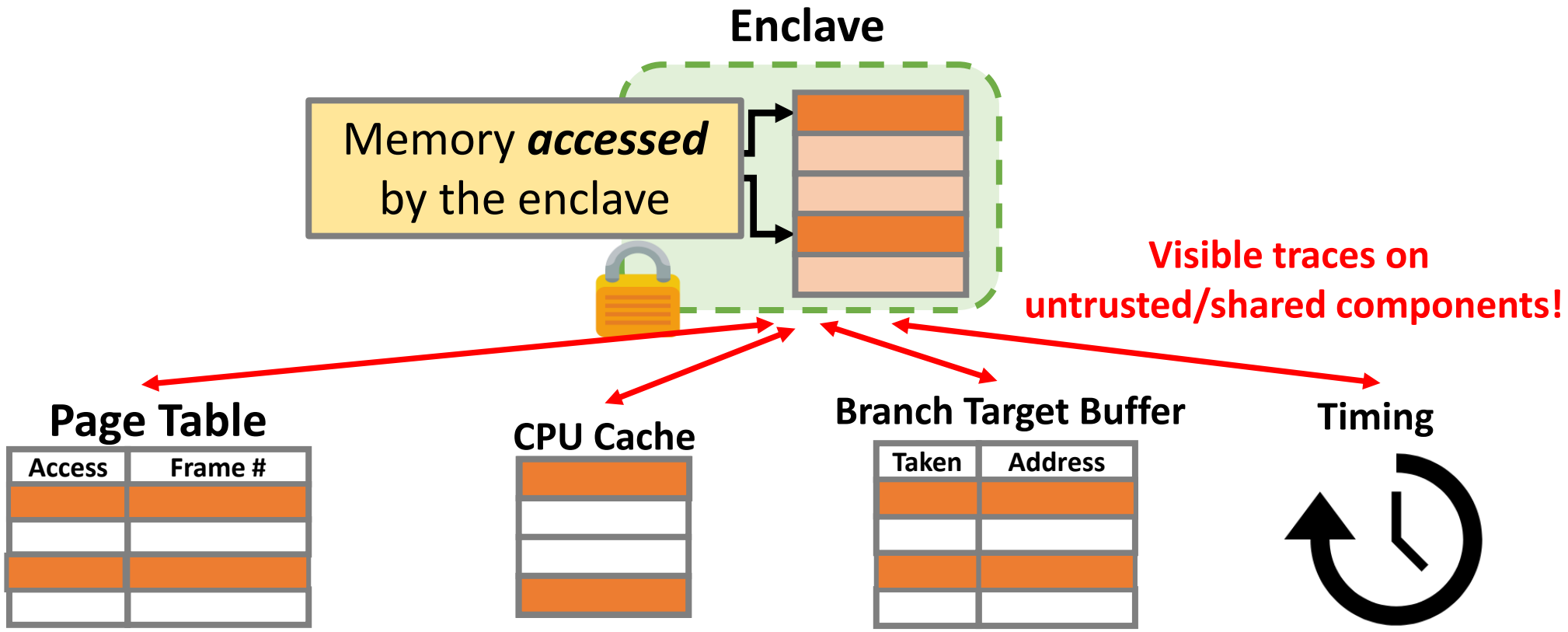

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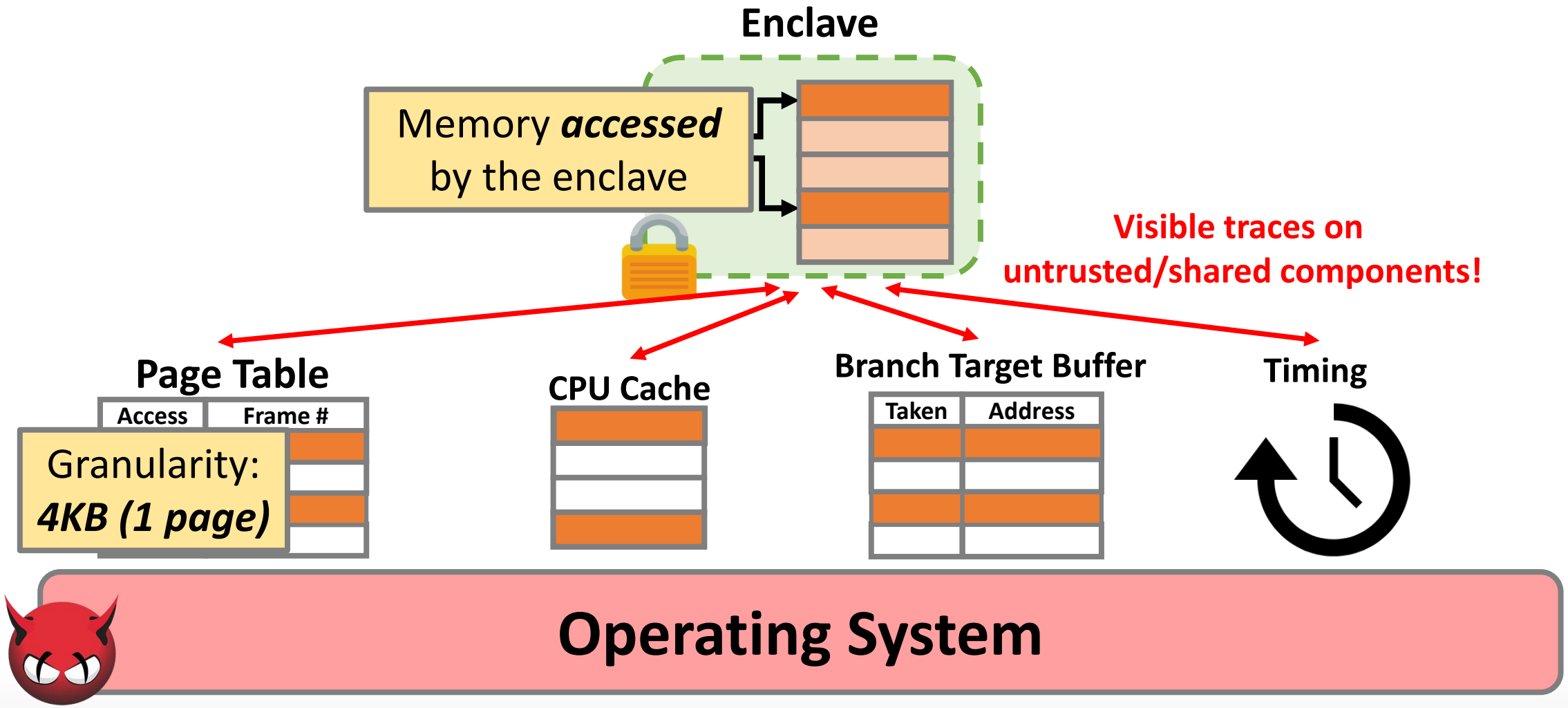

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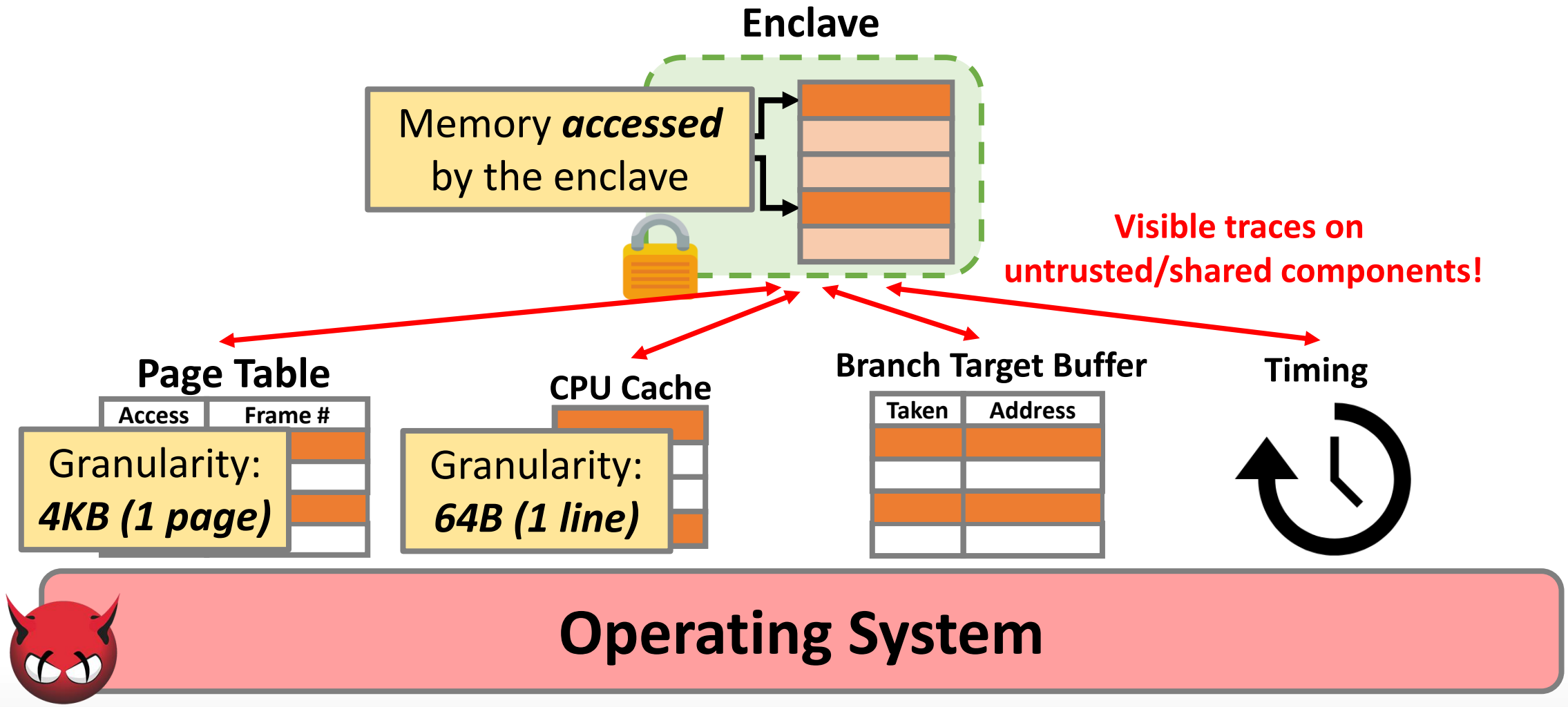

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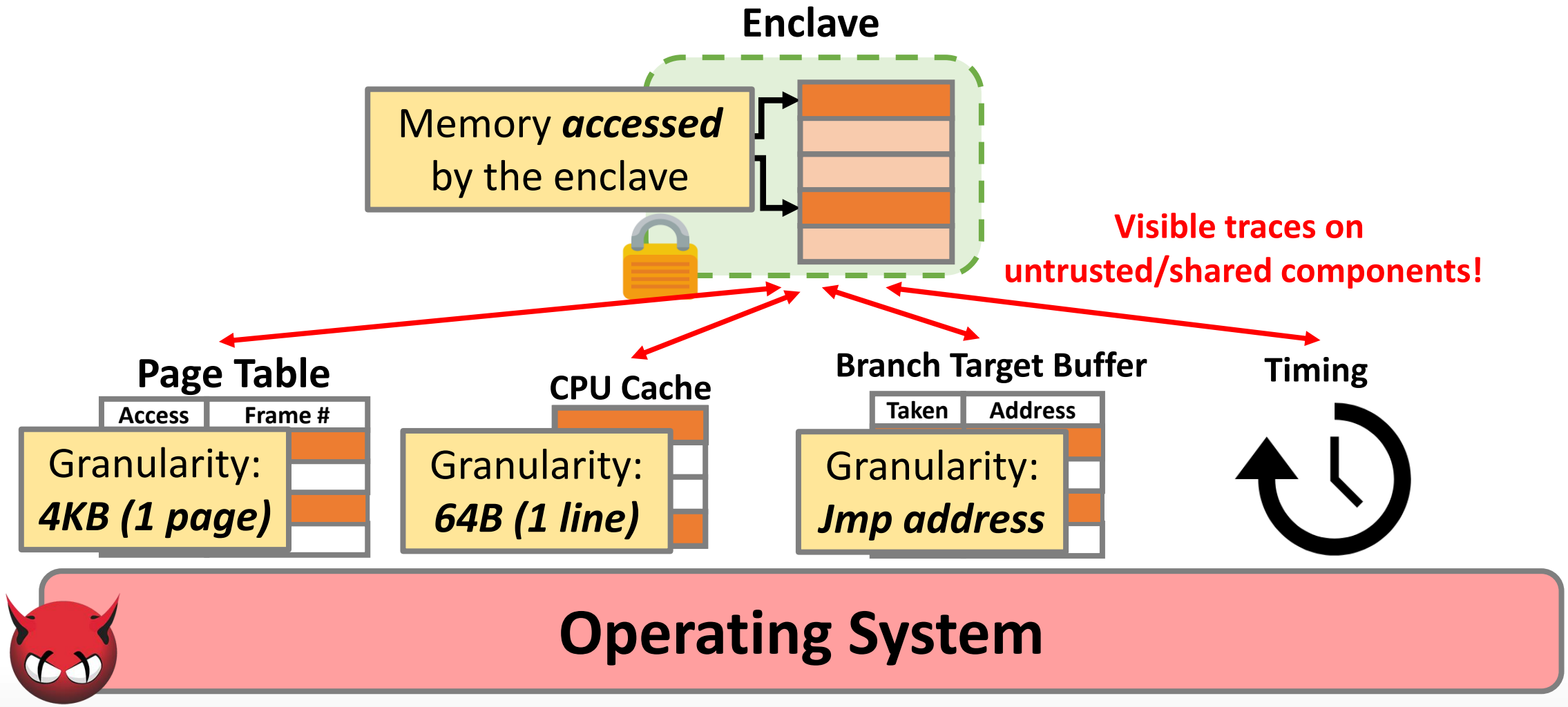

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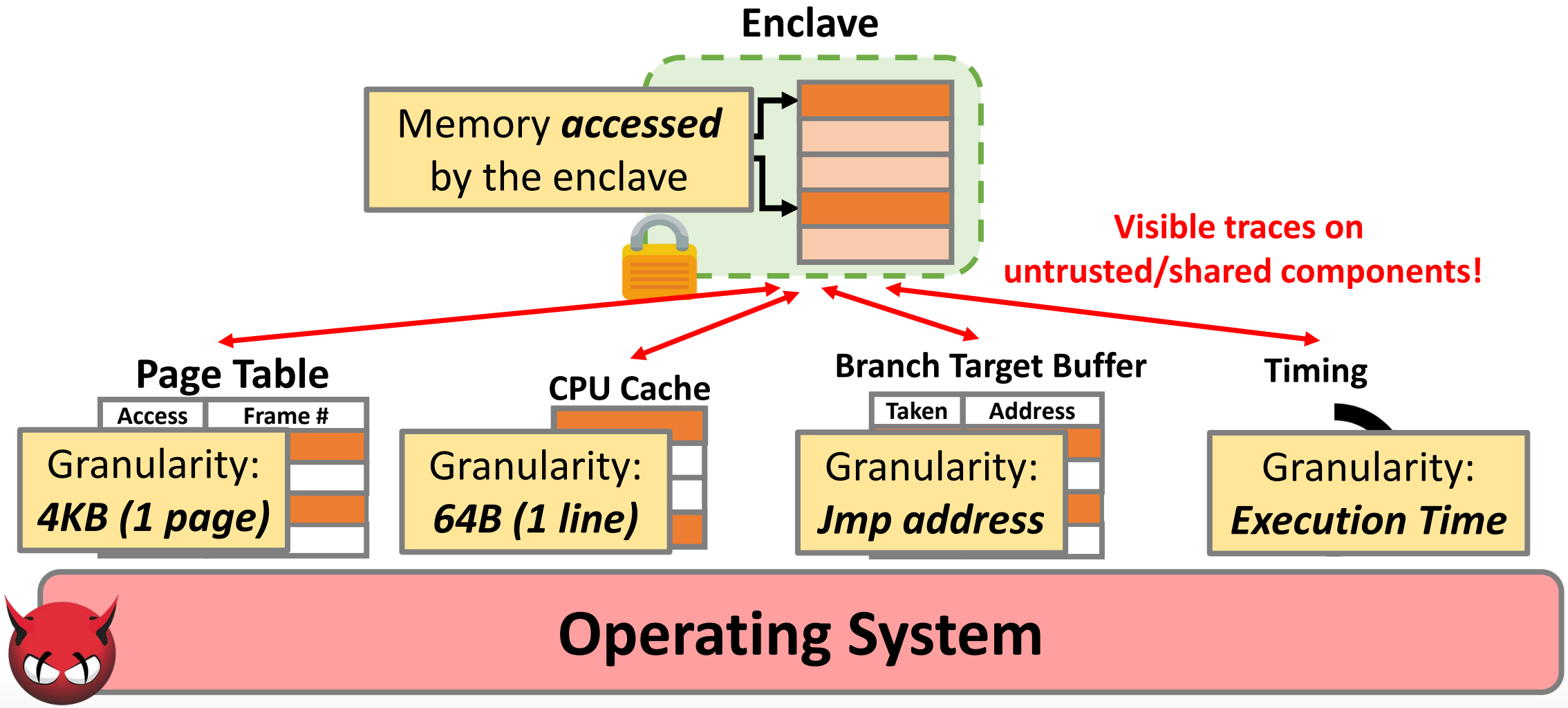

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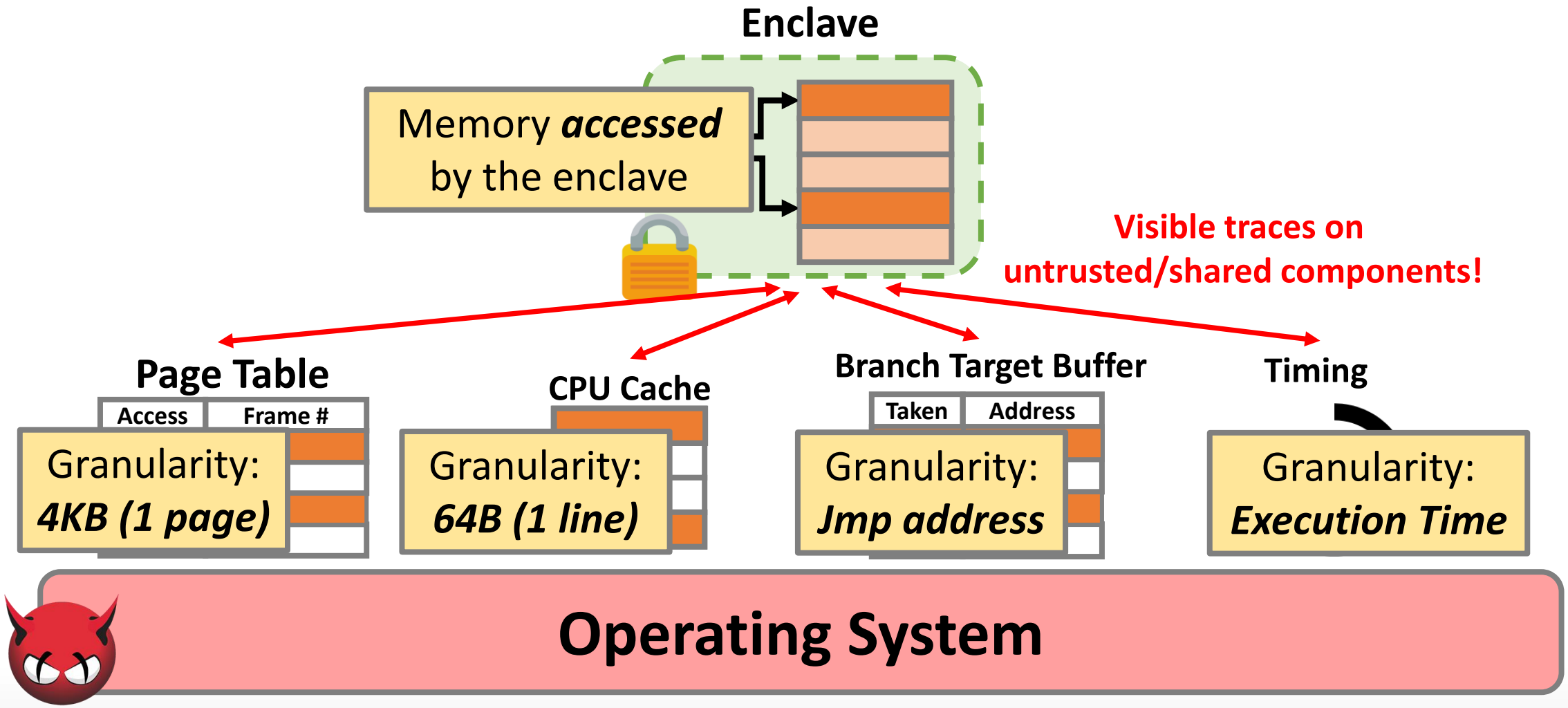

***Paging*, Branch-prediction** and **Cache attacks!**

[S&P14, SEC17, ASPLOS18, DIMVA17, WOOT17]

Learning from existing solutions!

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Access patterns attacks!

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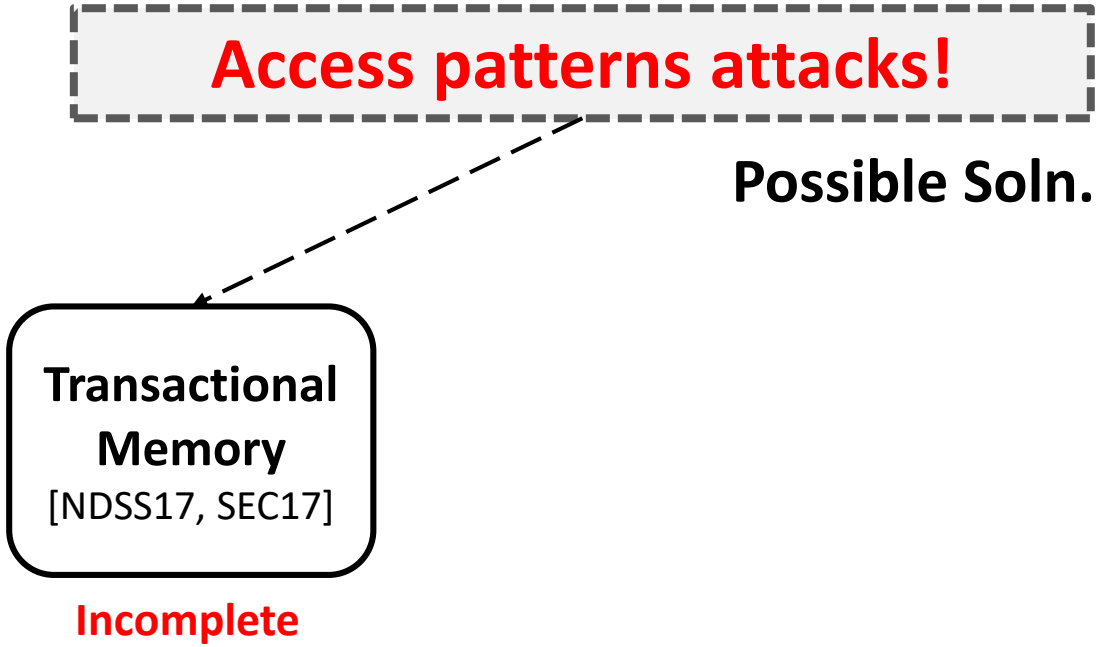

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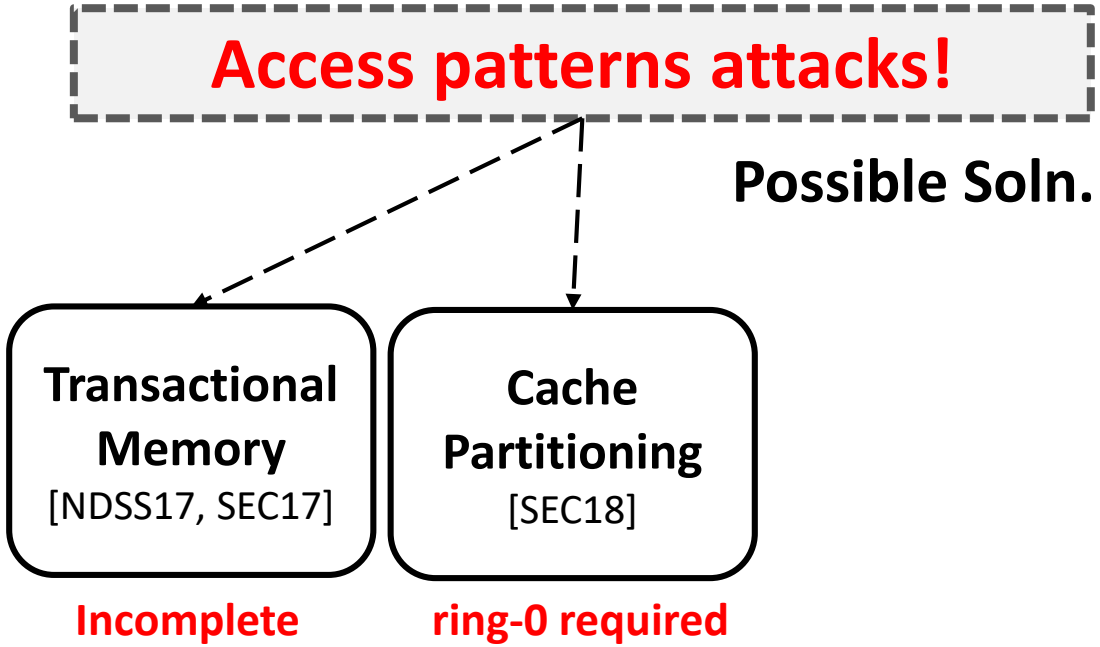

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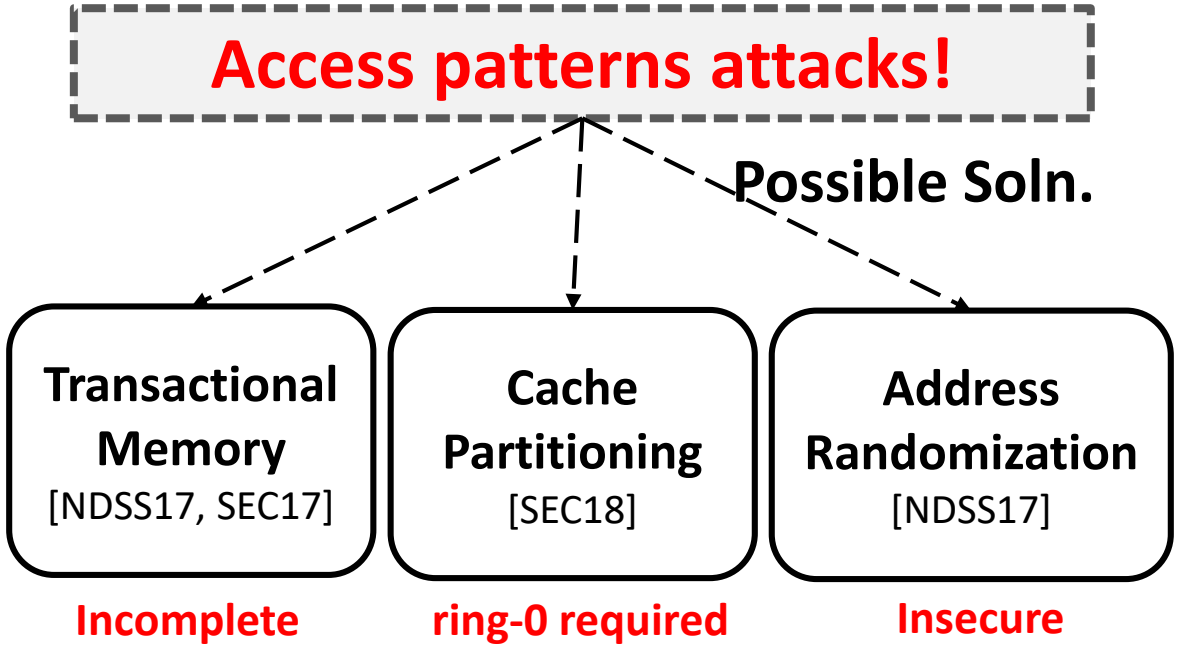

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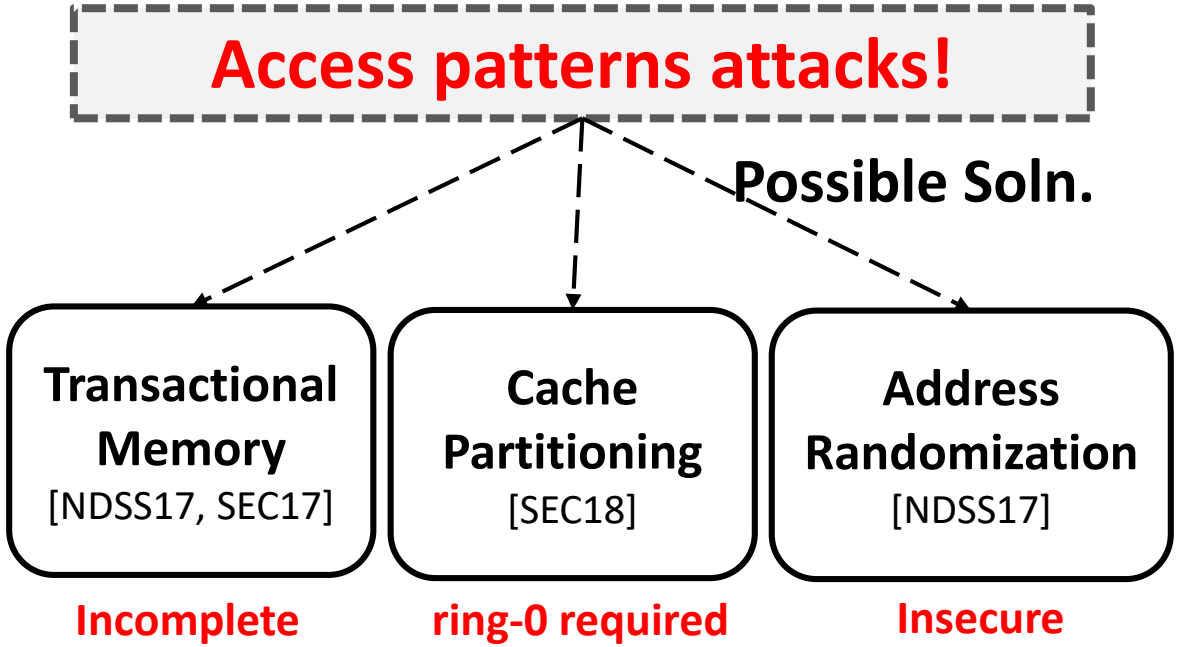

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Ring-3 enclaves cannot hide access patterns through side-channels!

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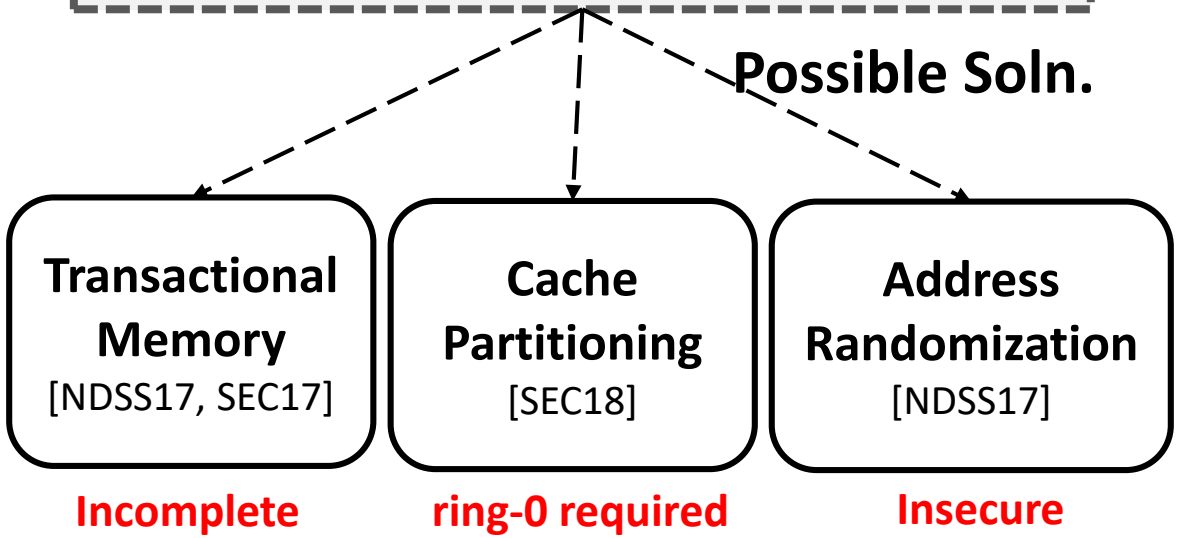

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Timing attacks!

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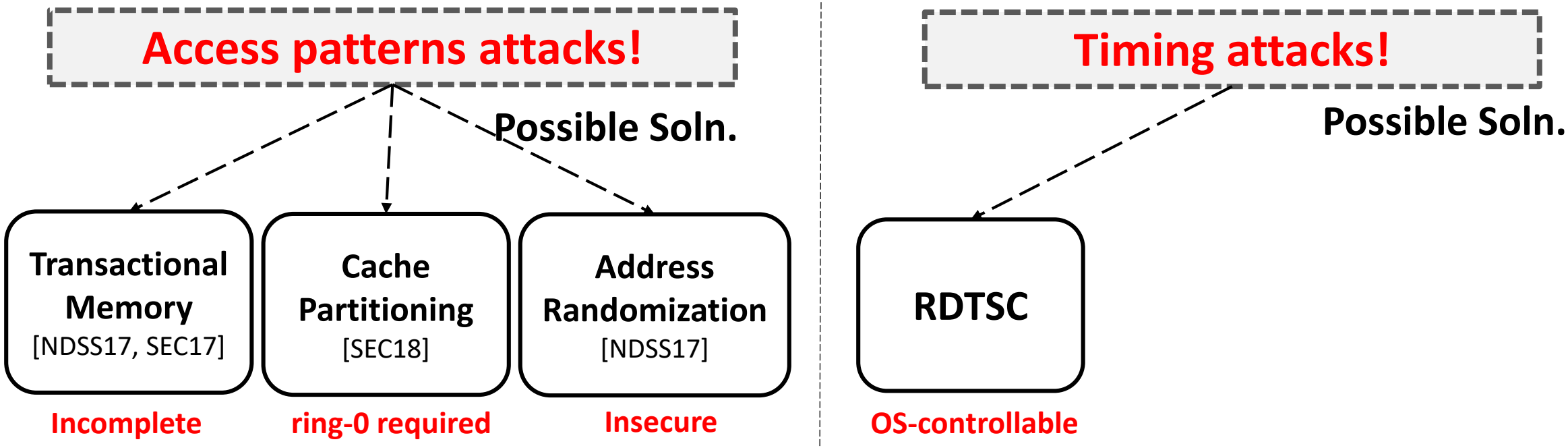

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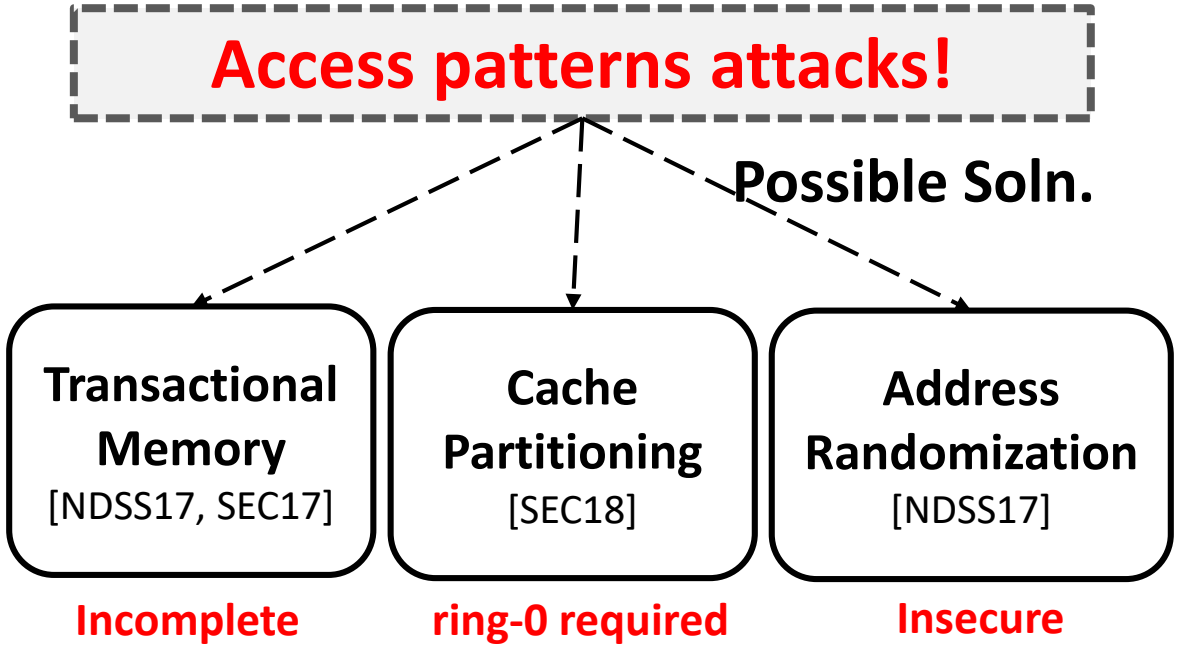

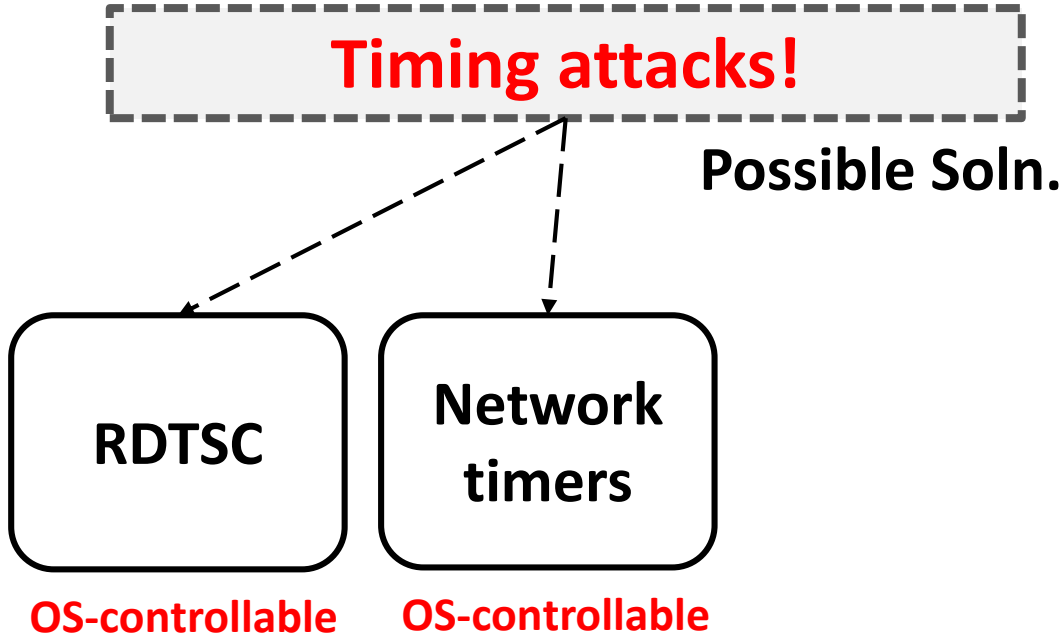

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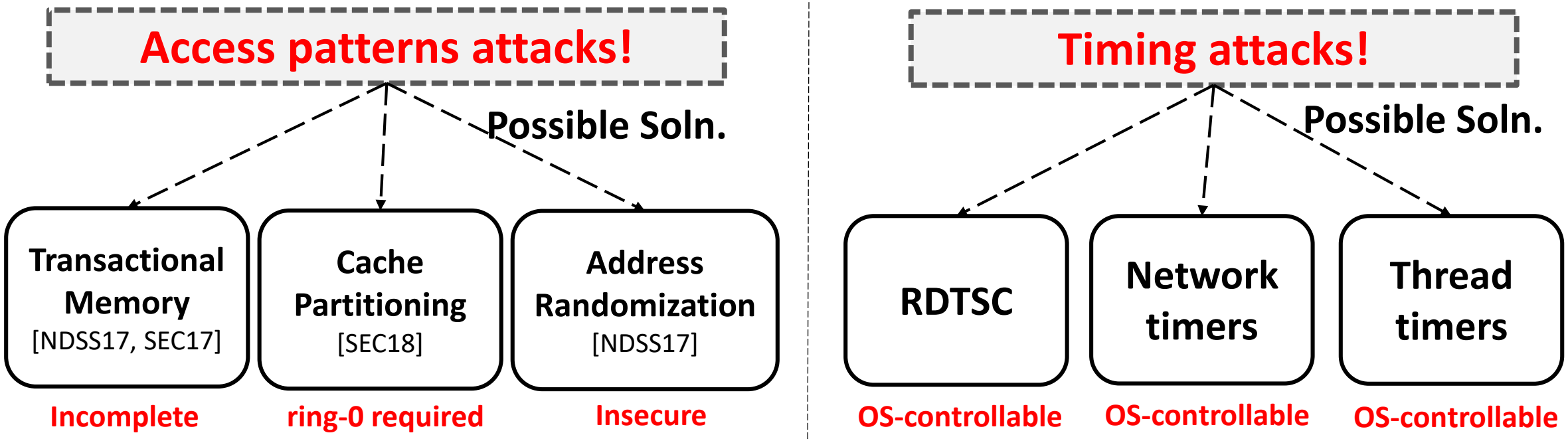

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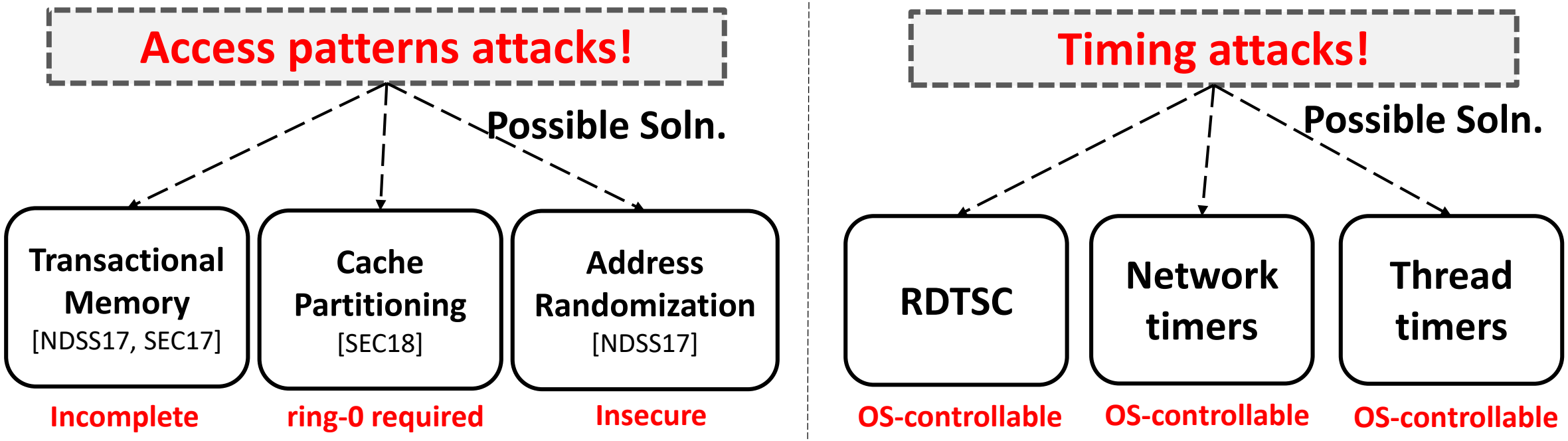

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Lesson #2

Unreliable timers for SGX enclaves!

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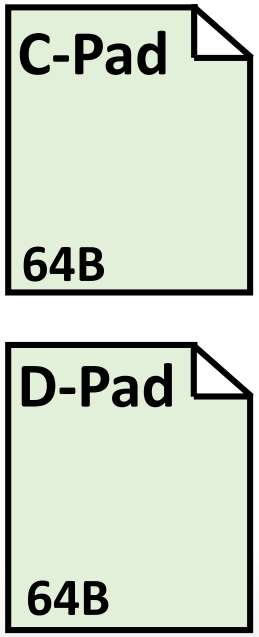

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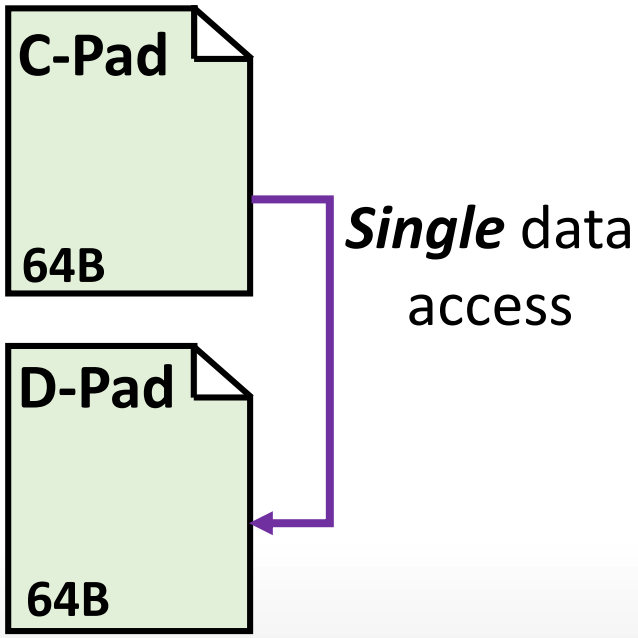

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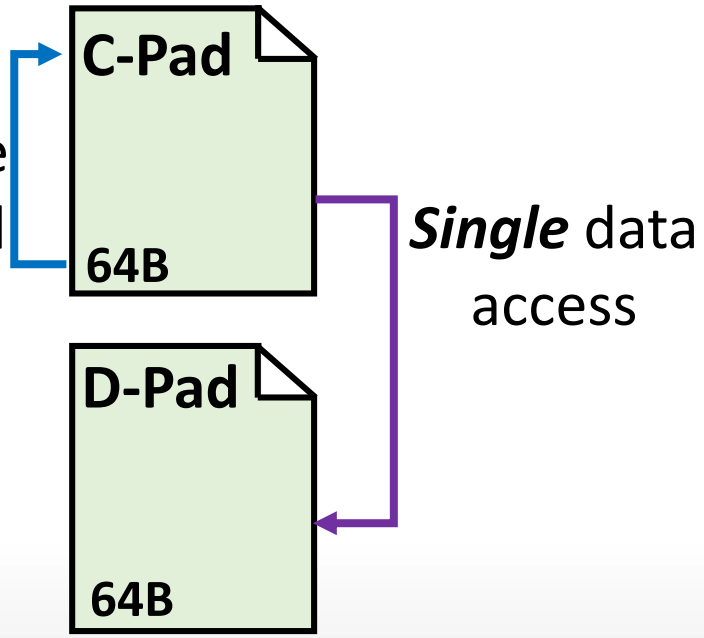

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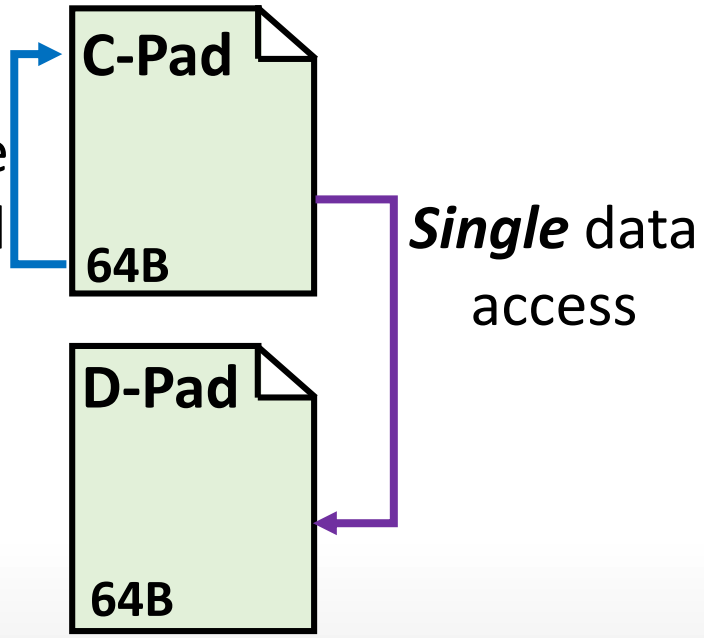

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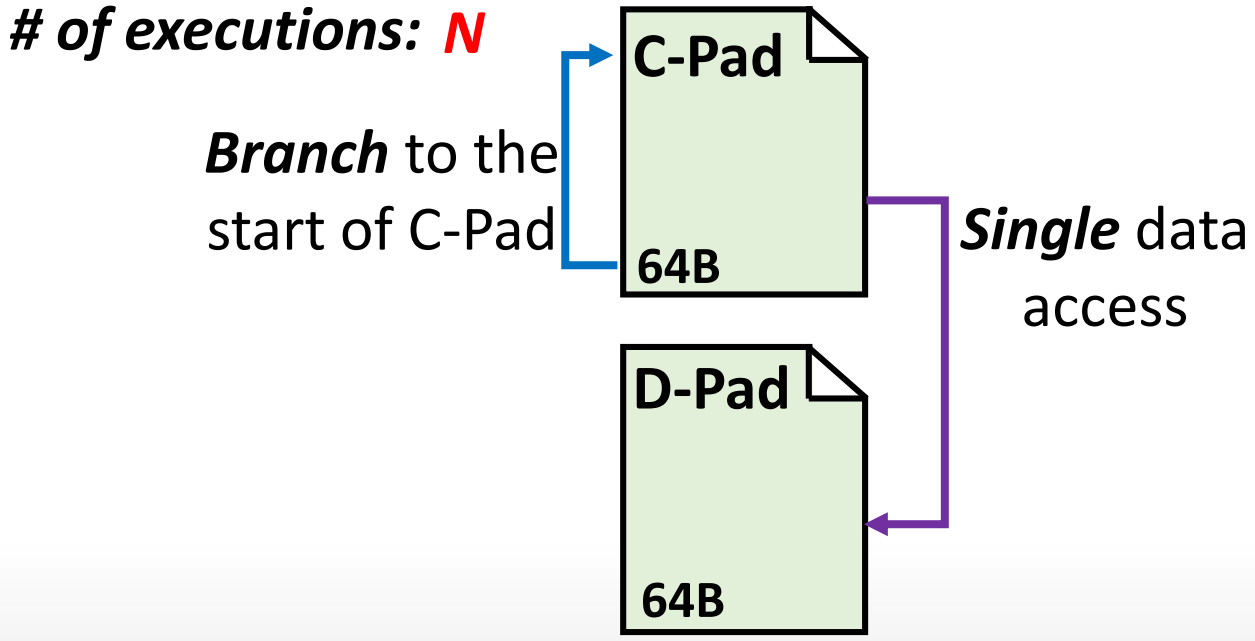

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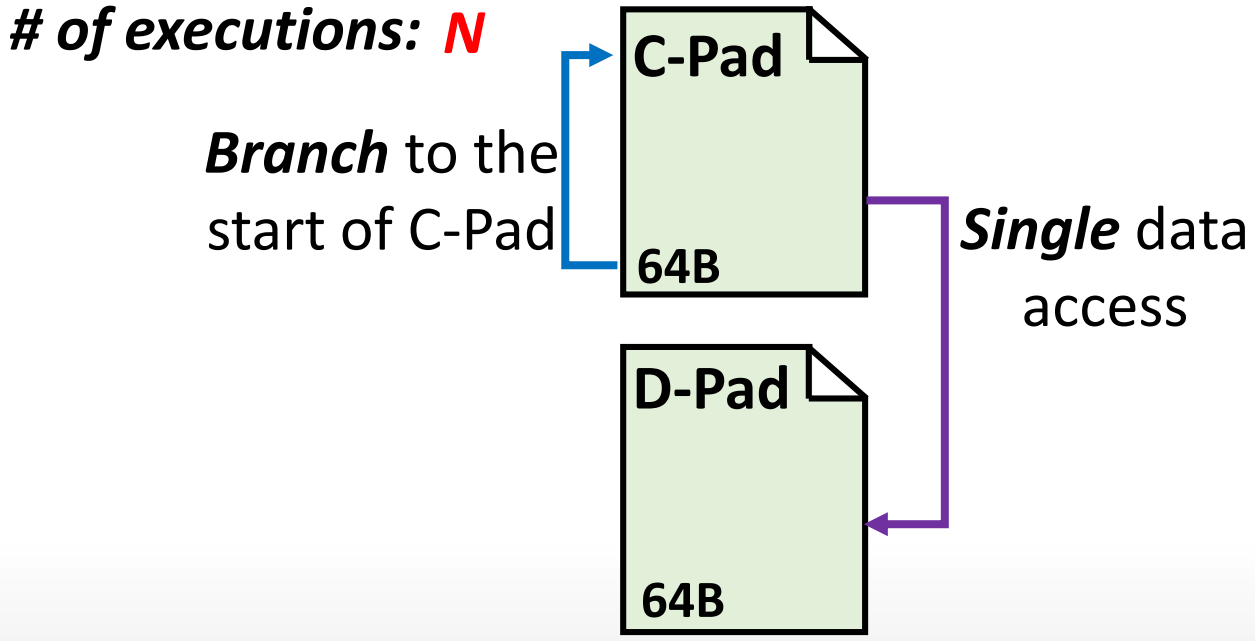

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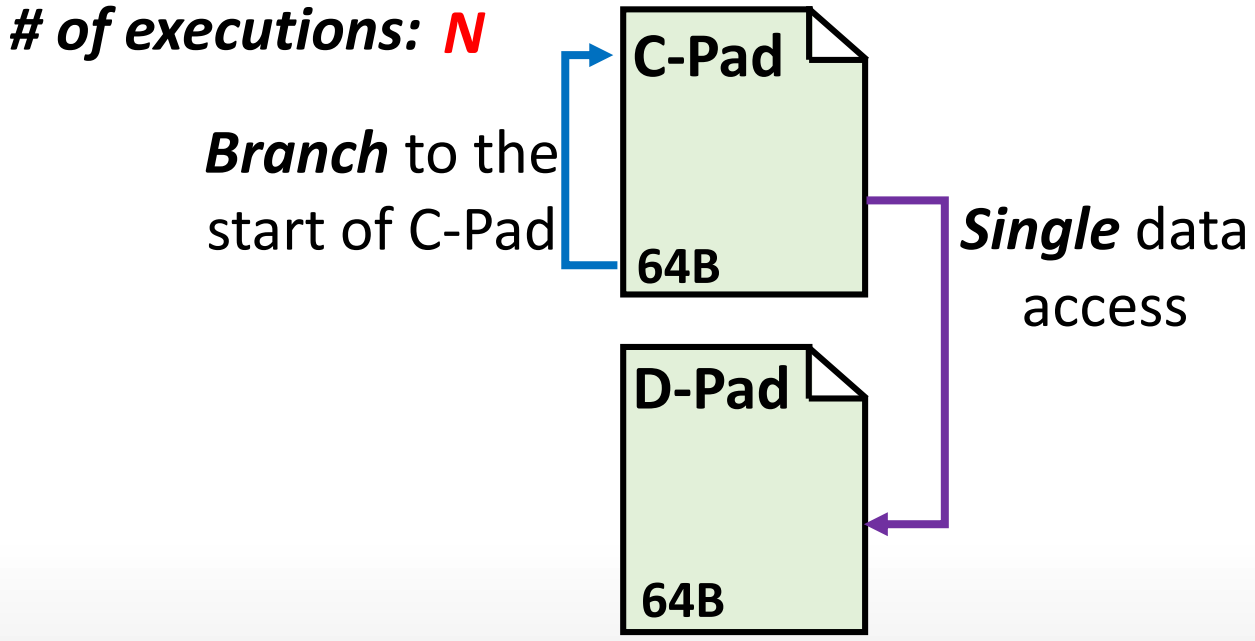

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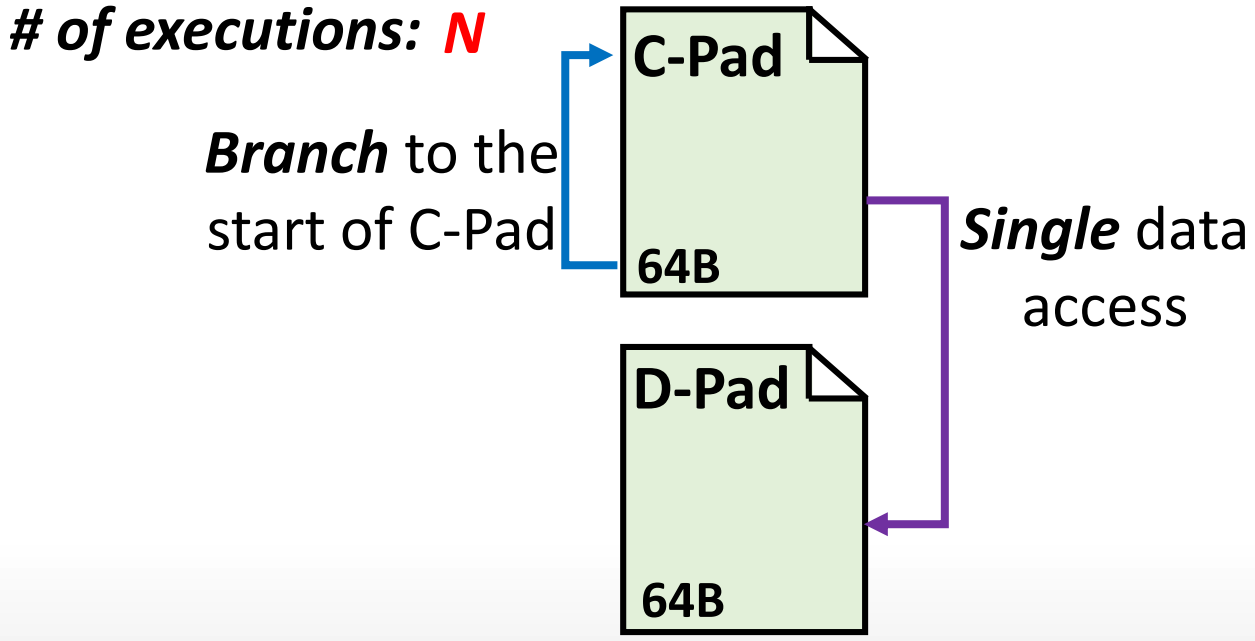

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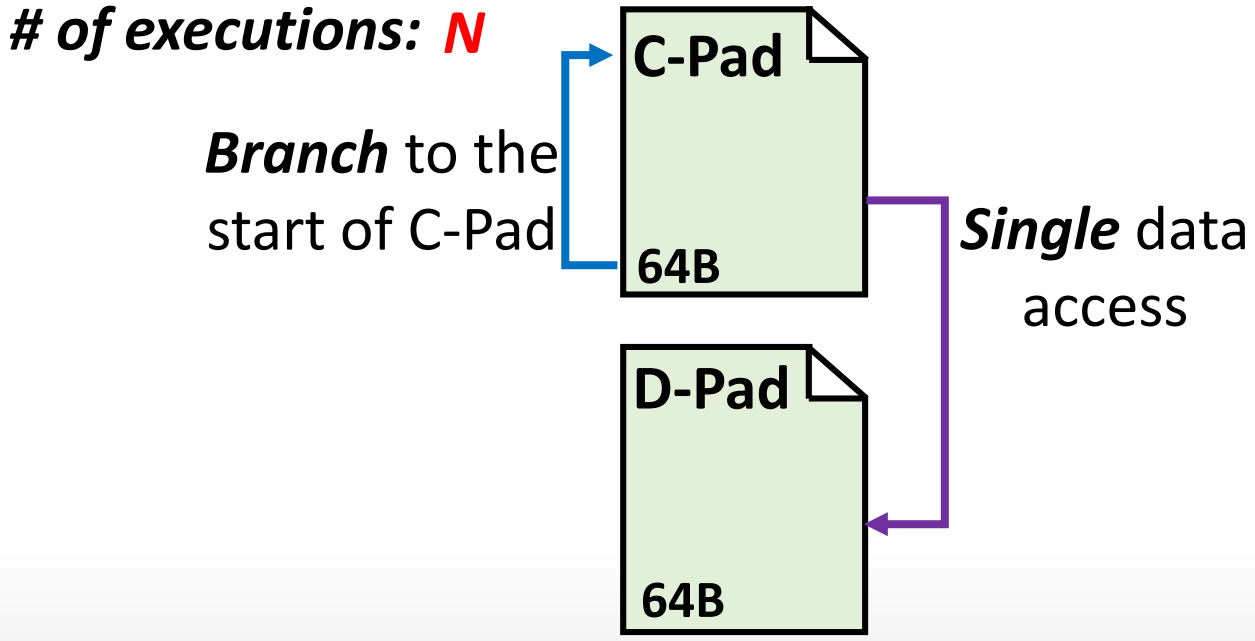

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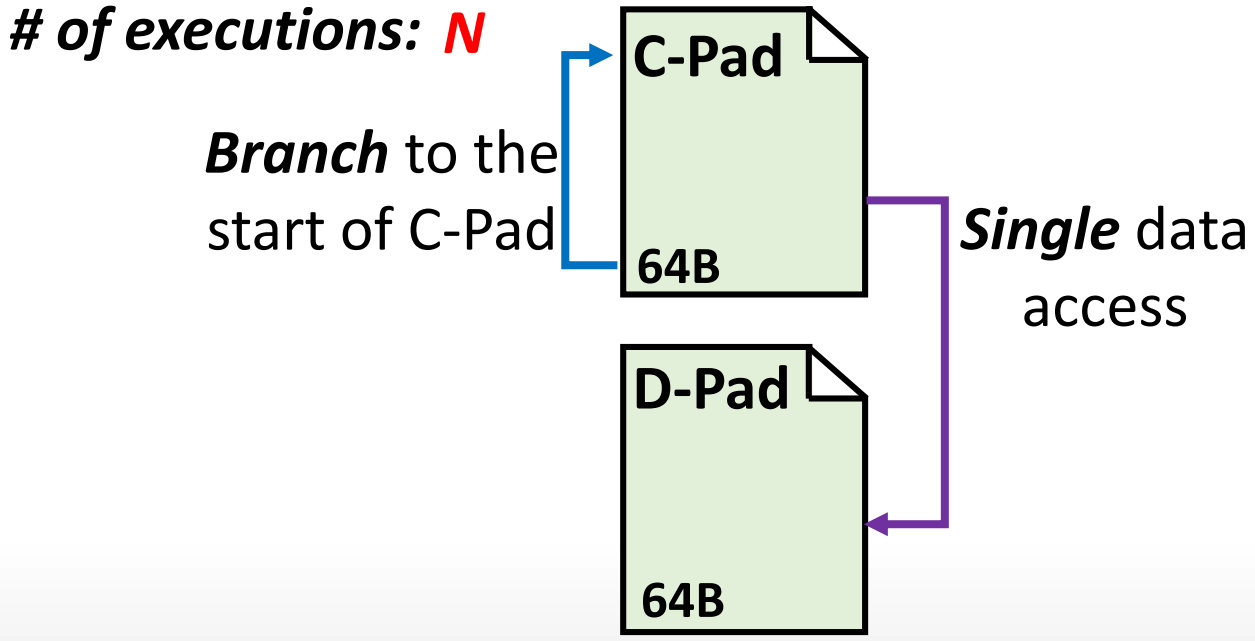

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Timing Attack: Same time to execute N code blocks

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Instead of ***trying to hide*** traces,
all enclaves should leak ***the same*** traces!

Cache Attack: Same cache-lines

Branch Attack: Same branch

Timing Attack: Same time to execute N code blocks

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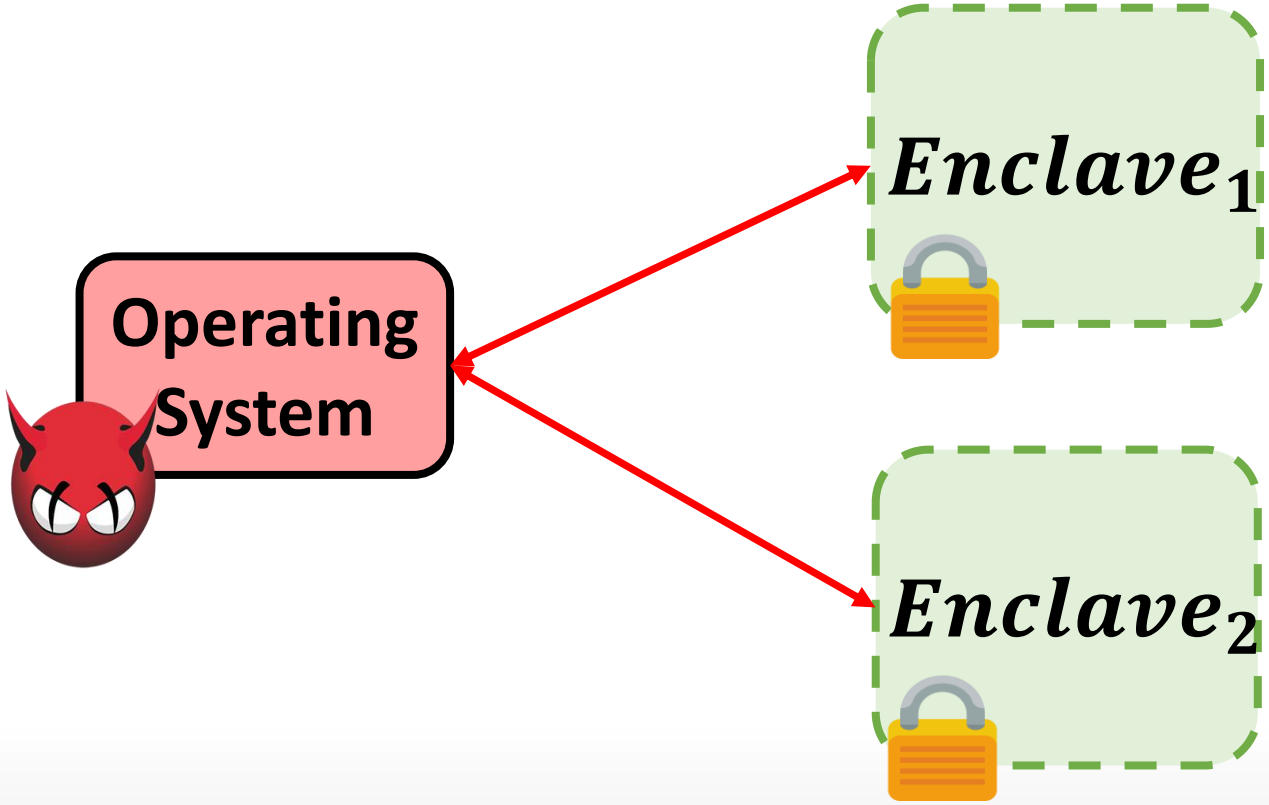

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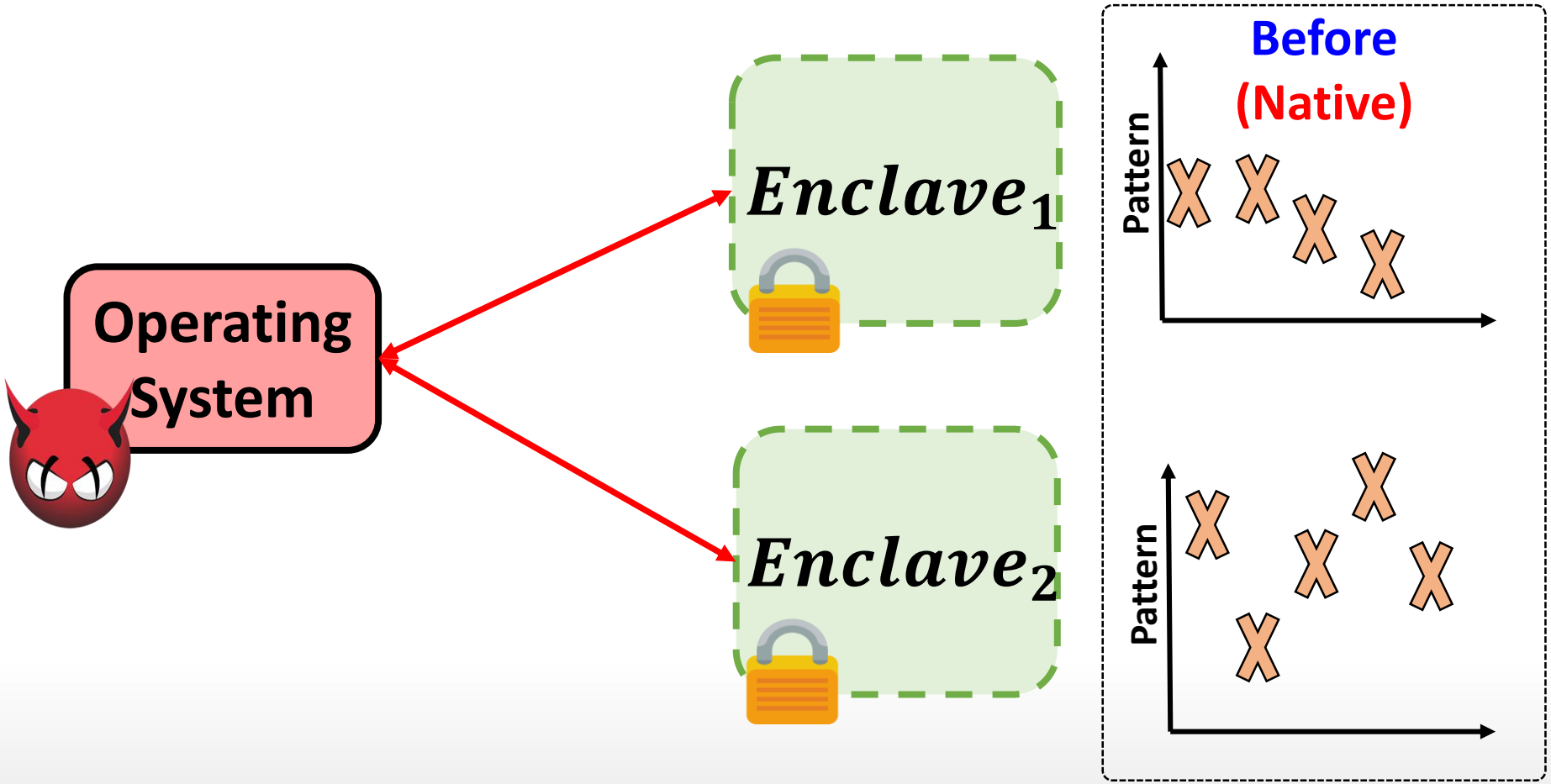

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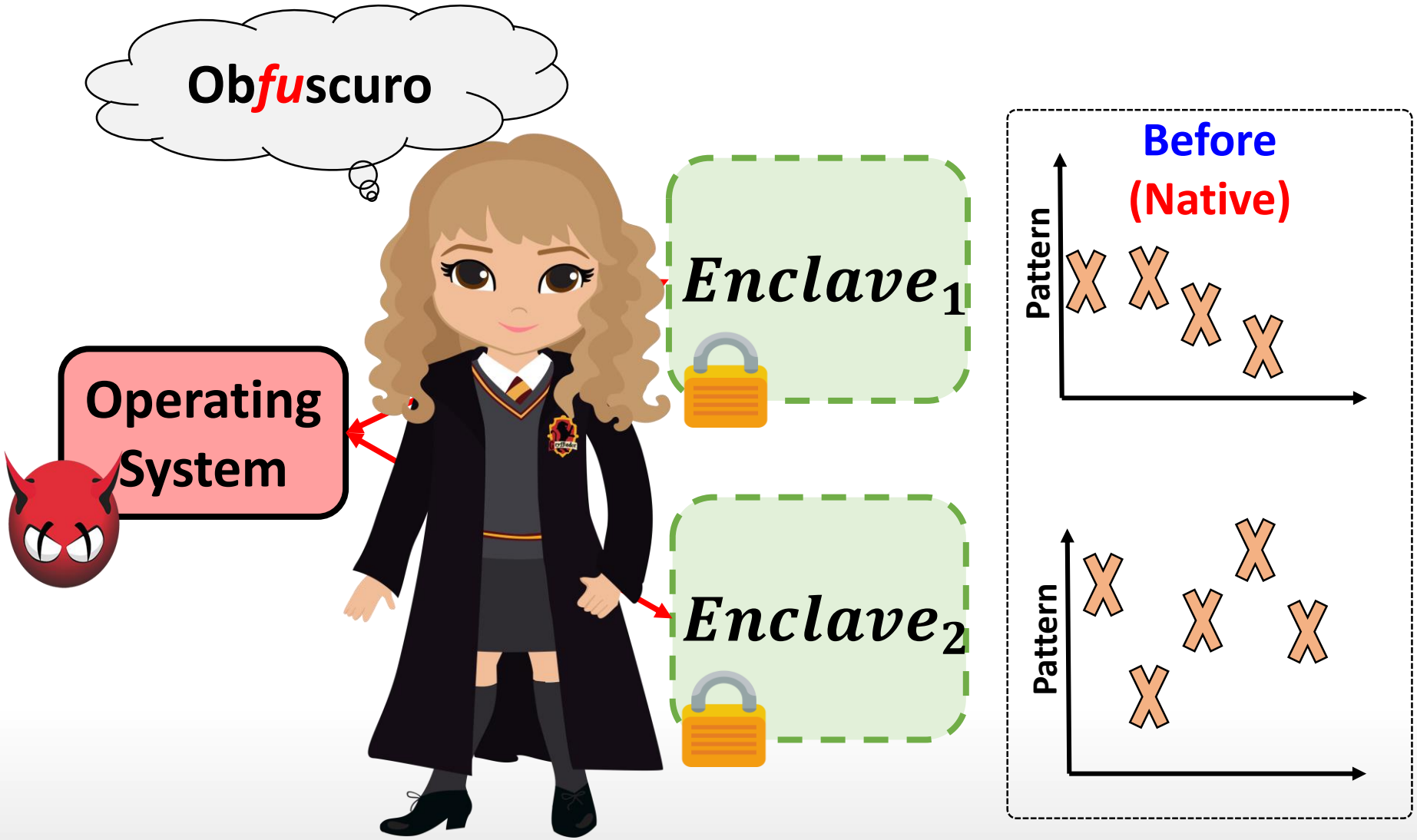

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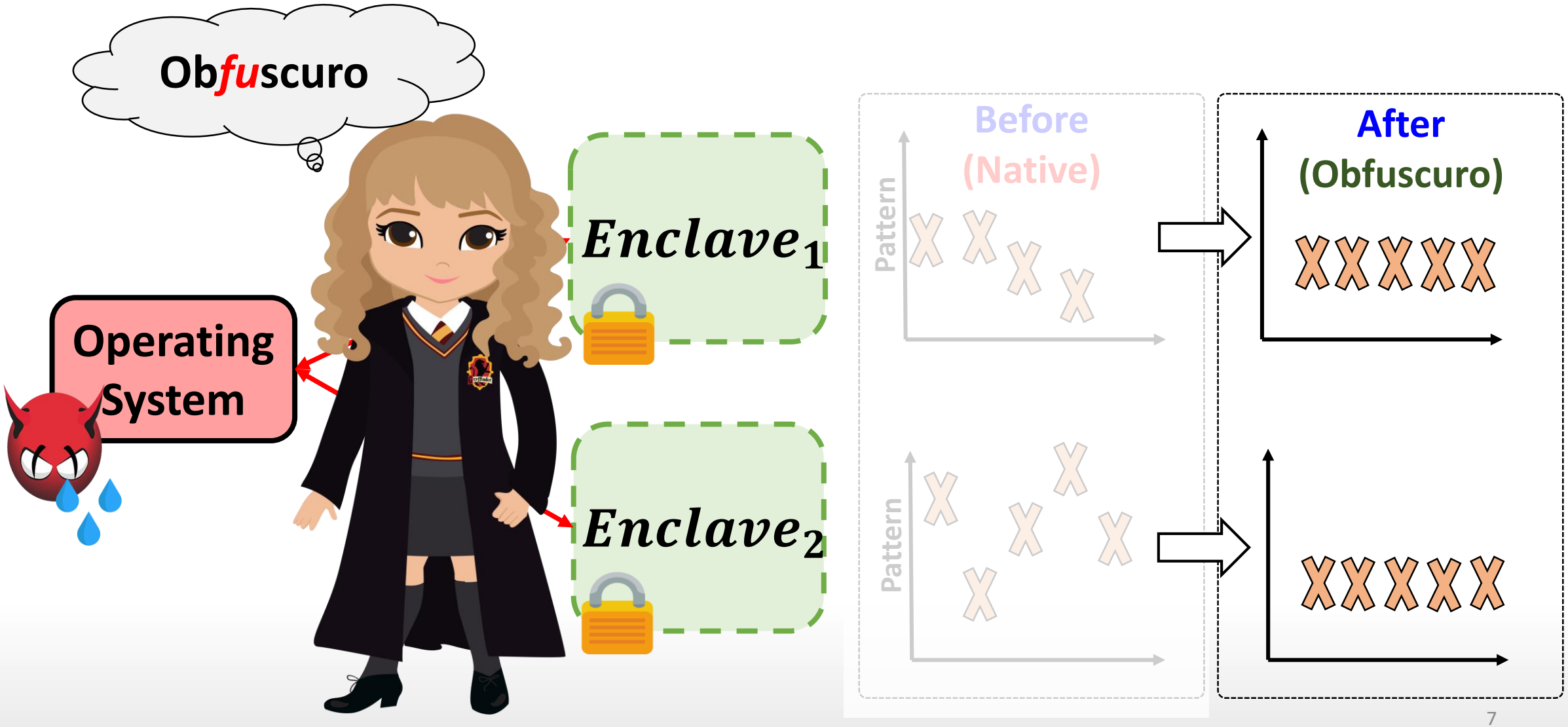

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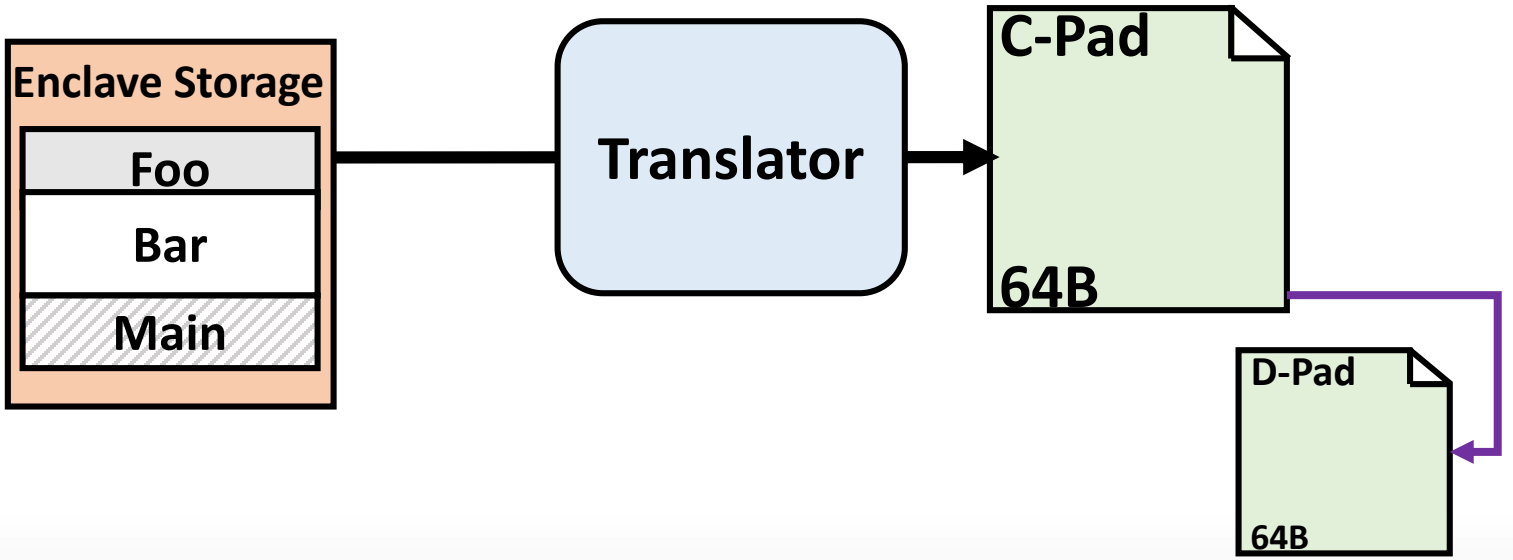

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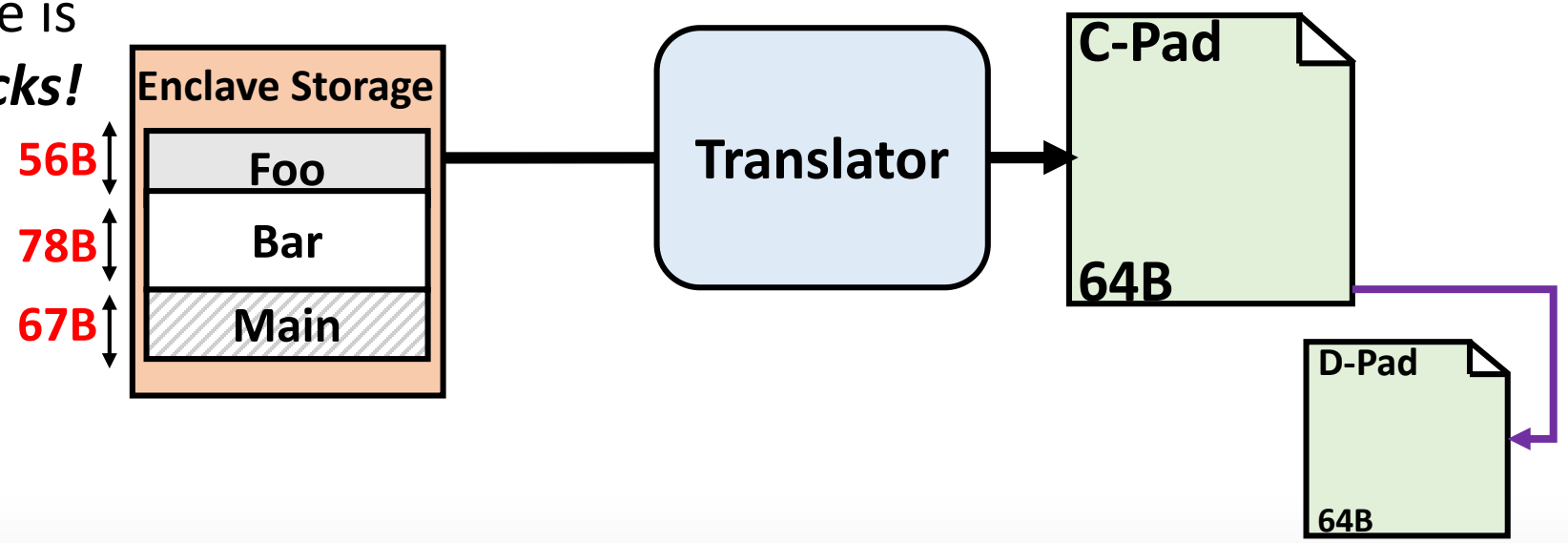

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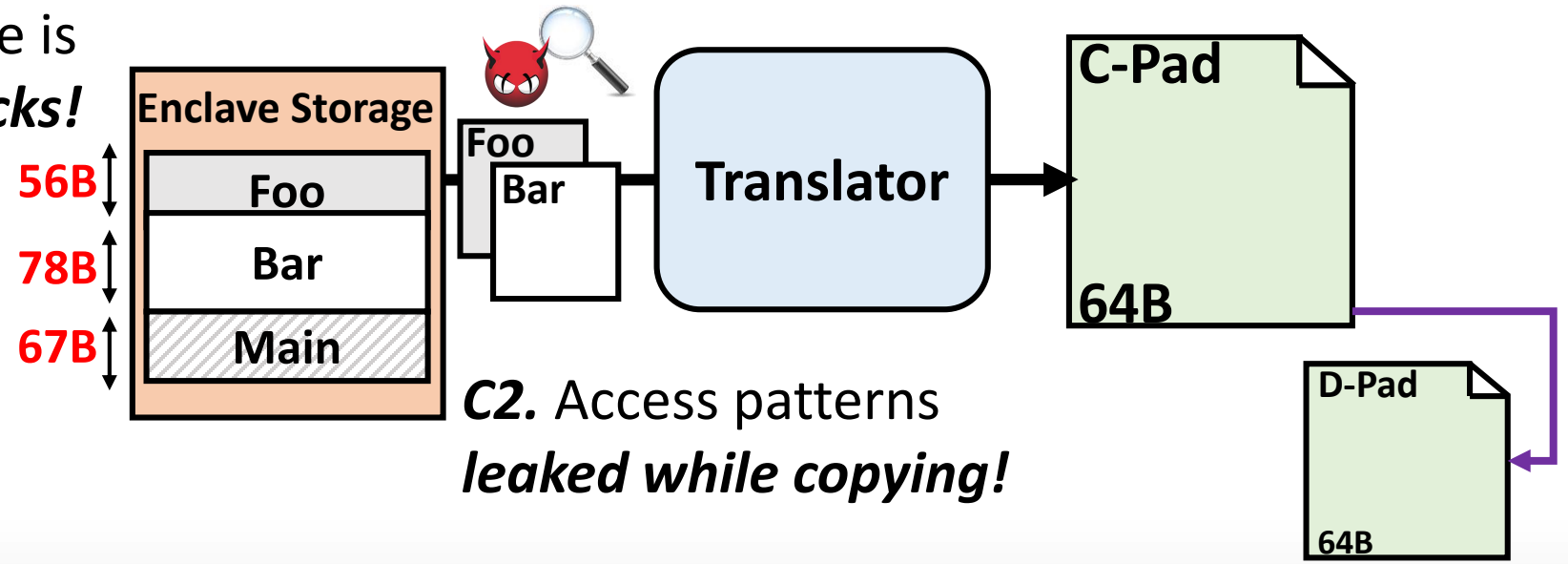

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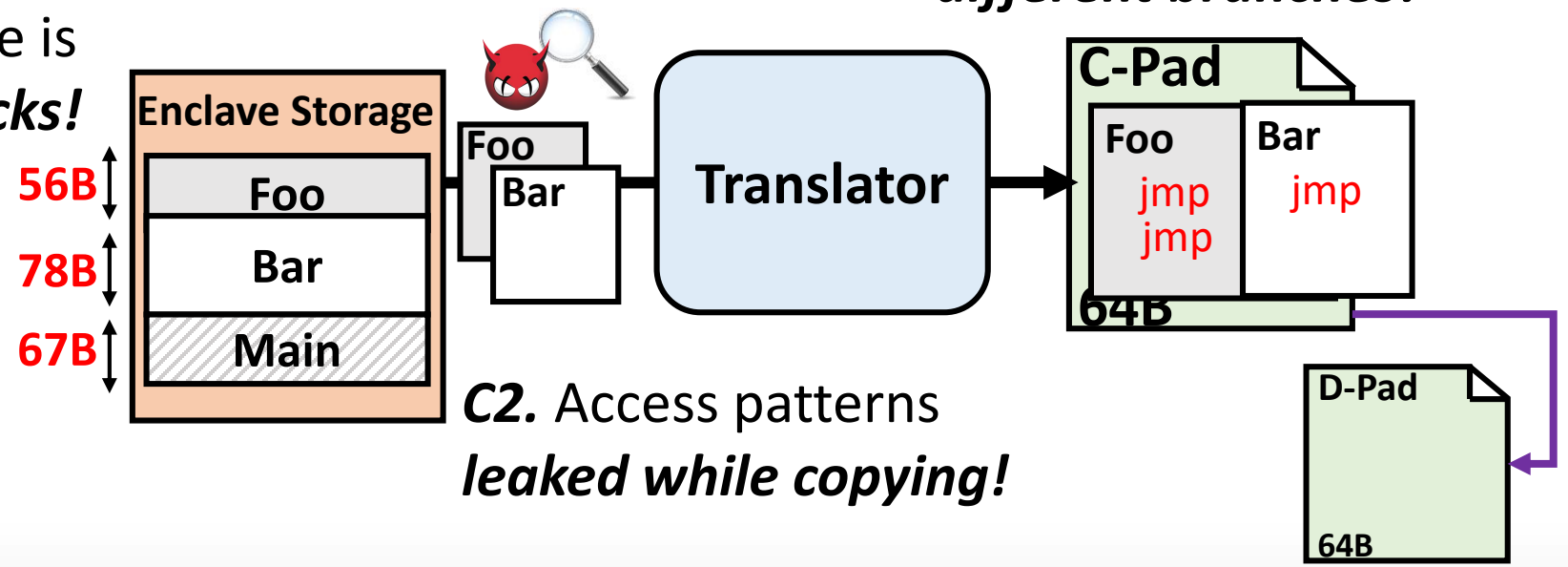

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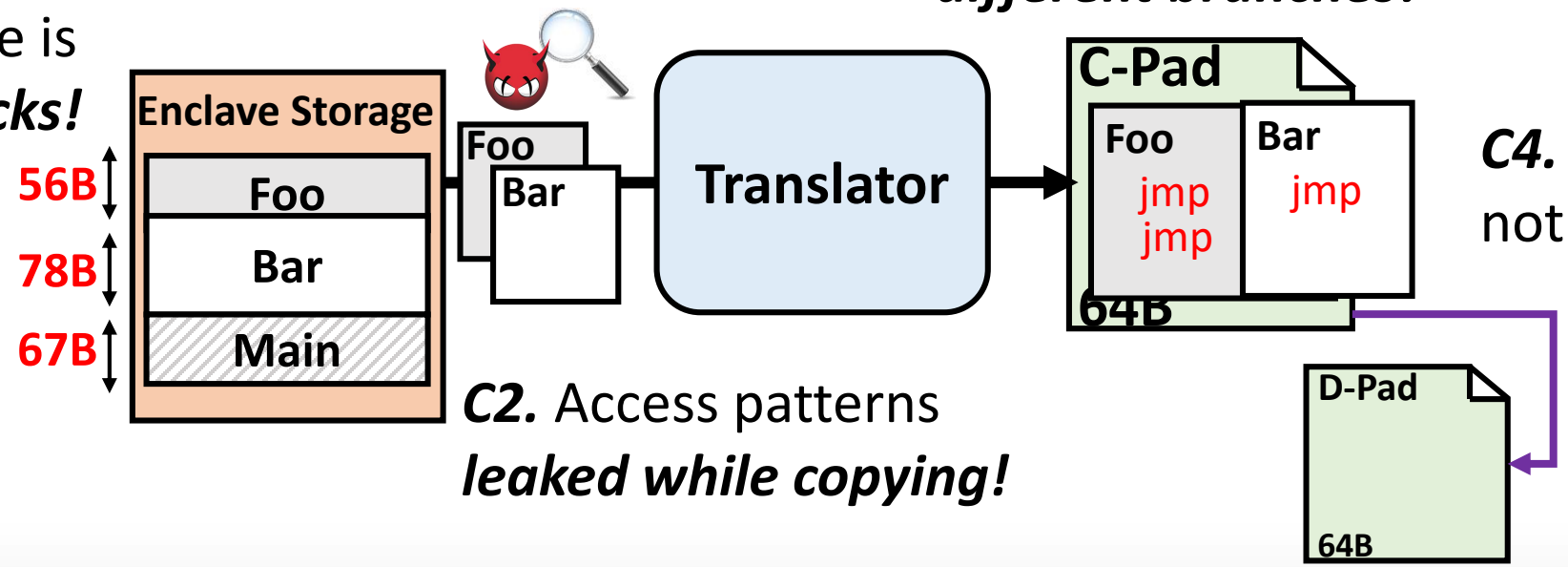

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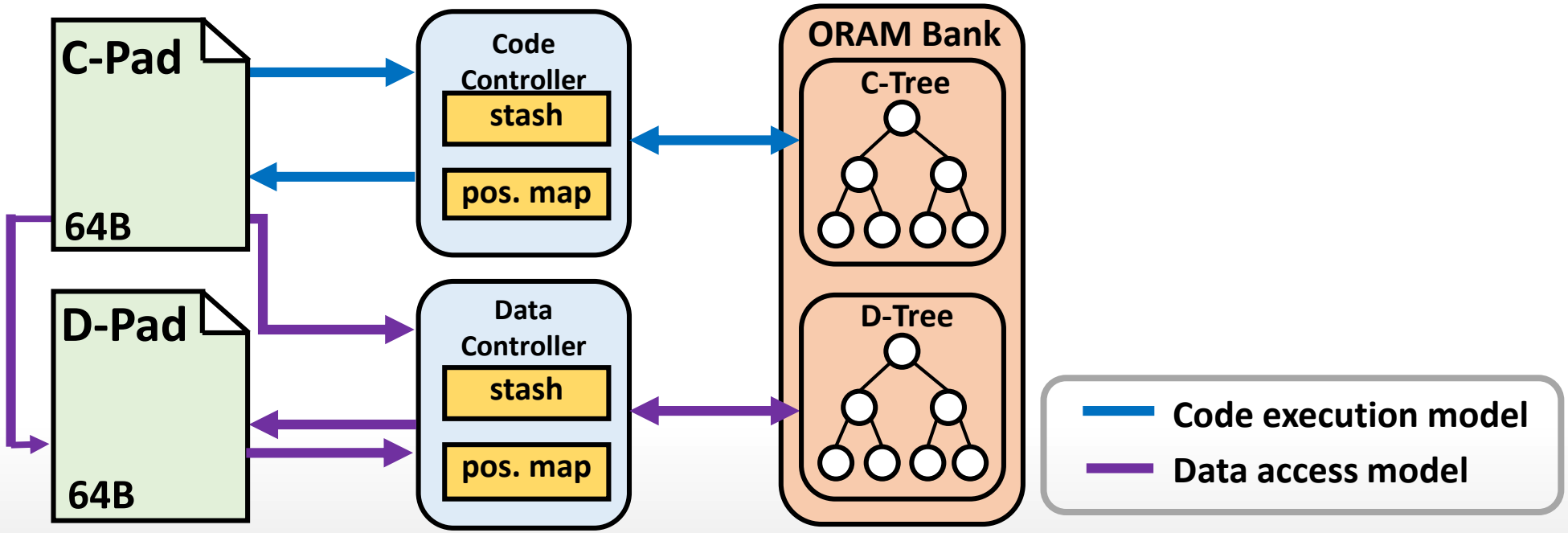
C4. Timing issues not even discussed!

Obfuscuro

- **Program obfuscation on Intel SGX**
  - All programs should exhibit same patterns irrespective of logic/input.
  - Adapted from Harry Potter spell "Obscuro" **(translation :> Darkness)**



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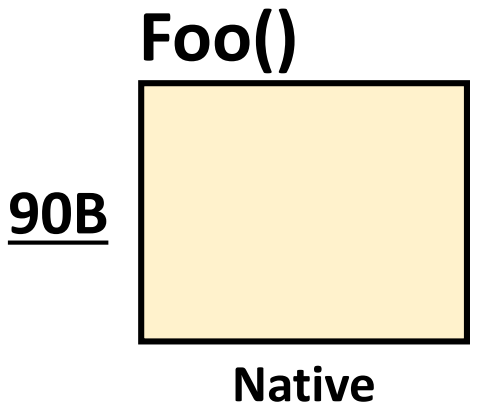

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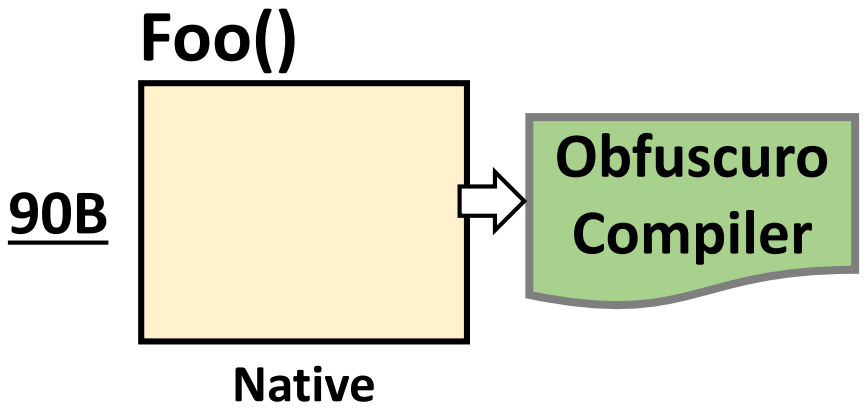

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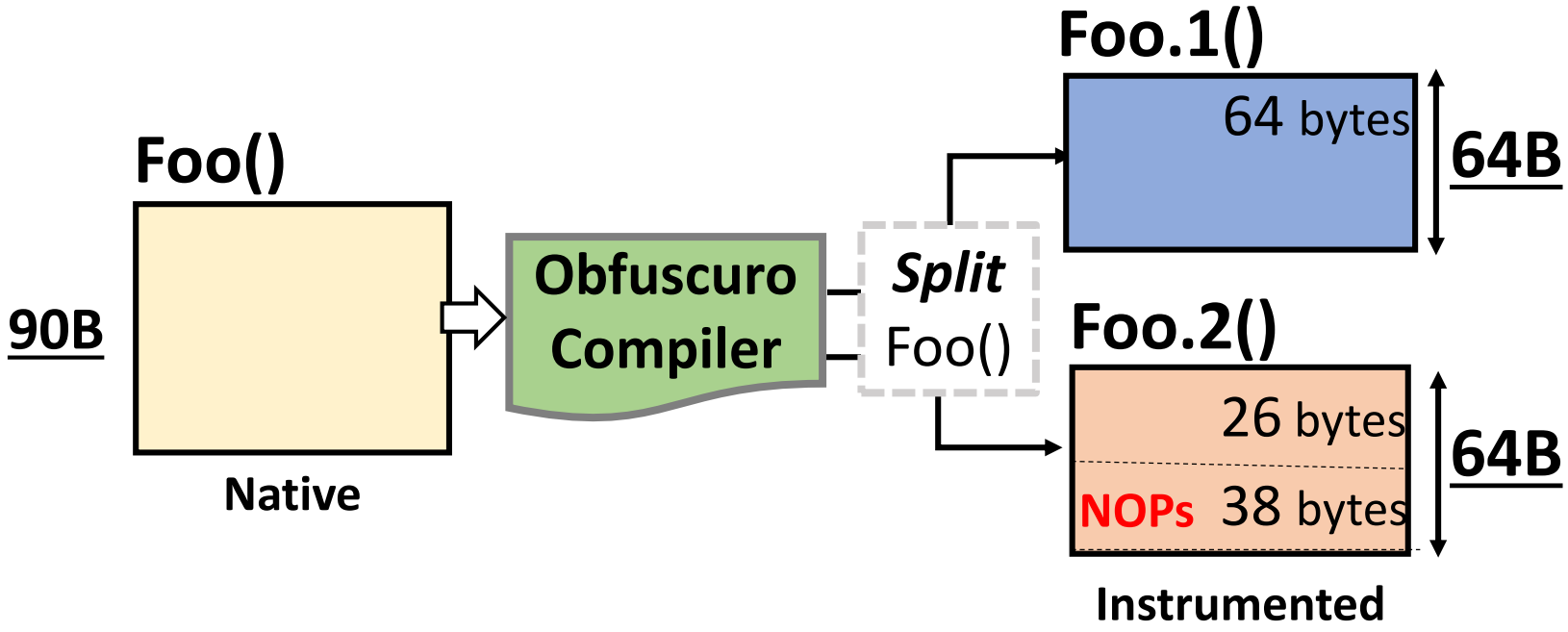

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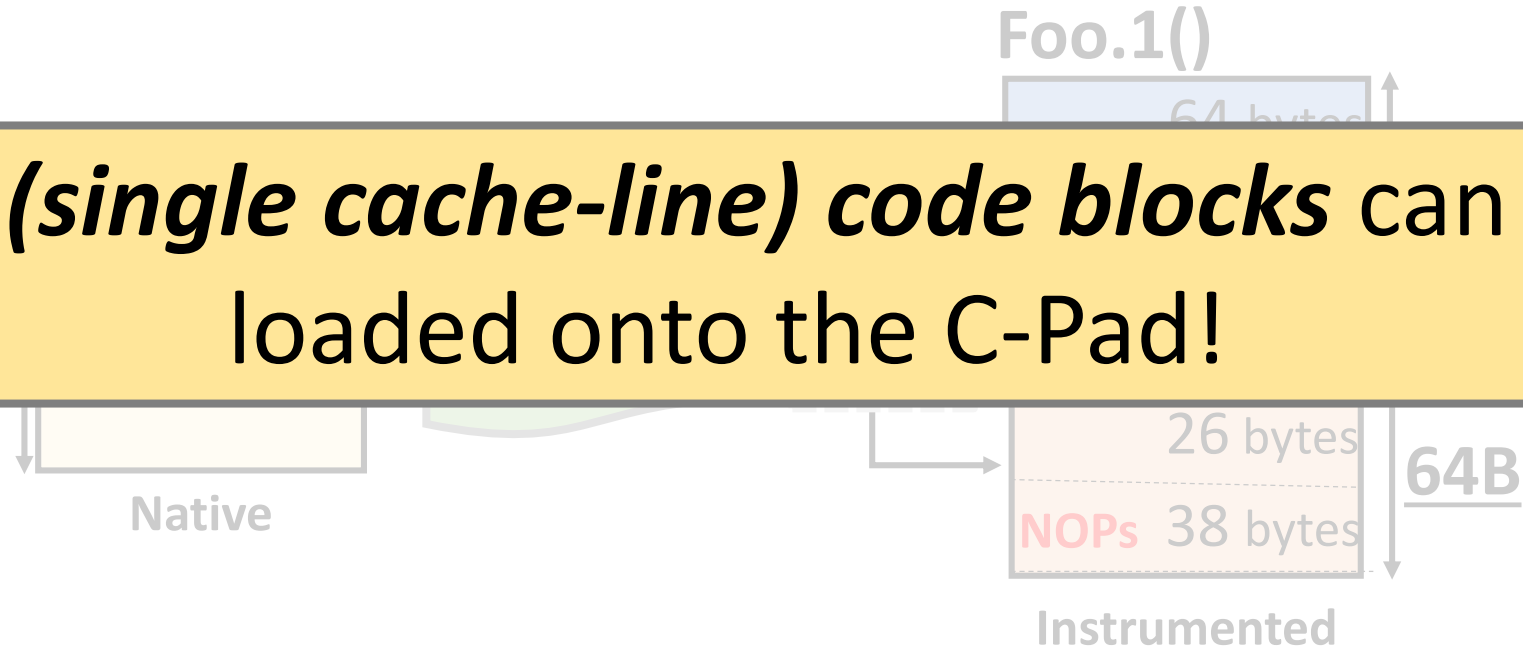

64B (single cache-line) code blocks can be loaded onto the C-Pad!

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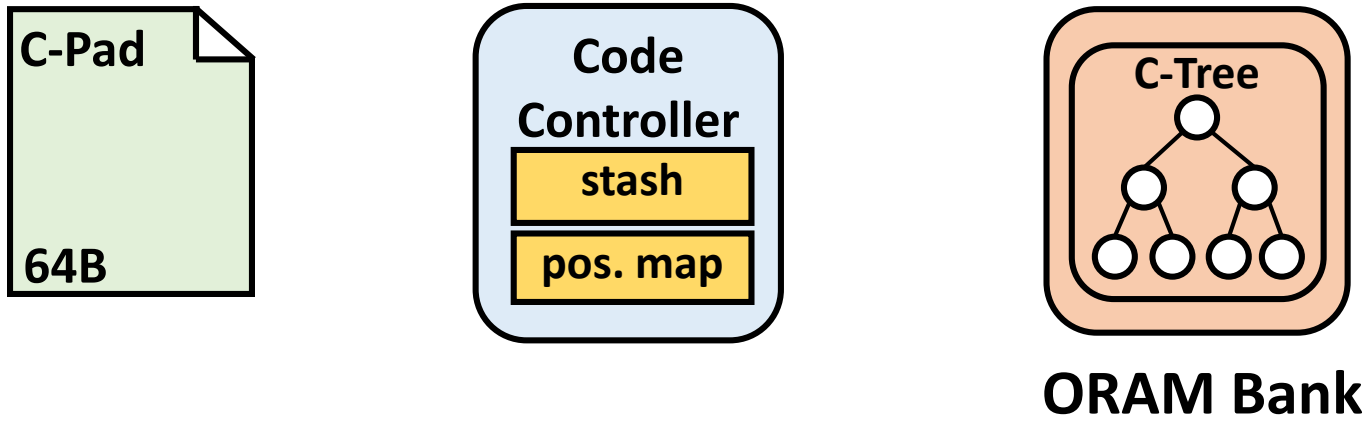

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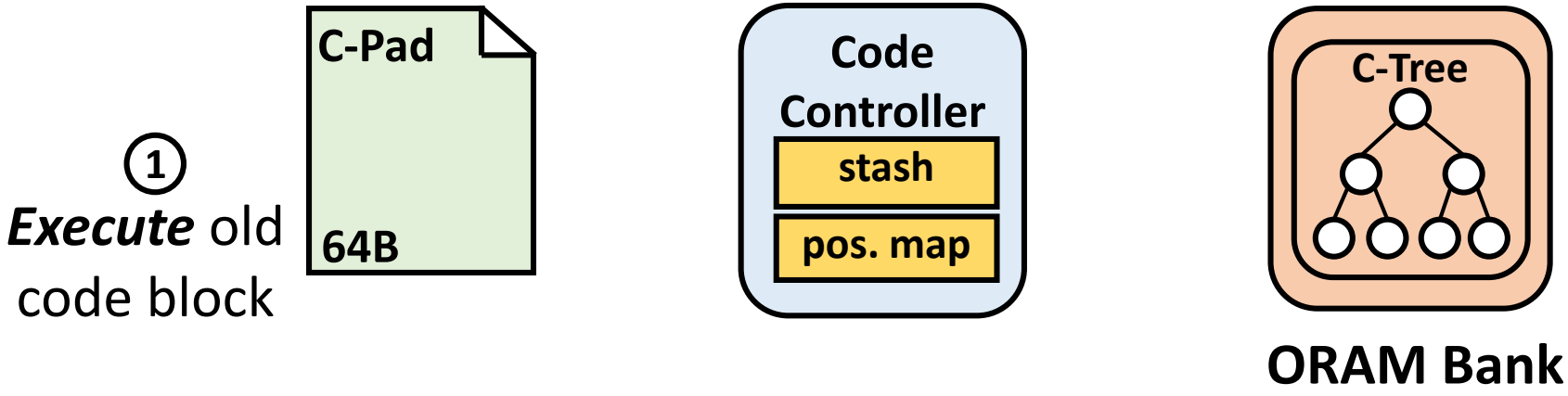

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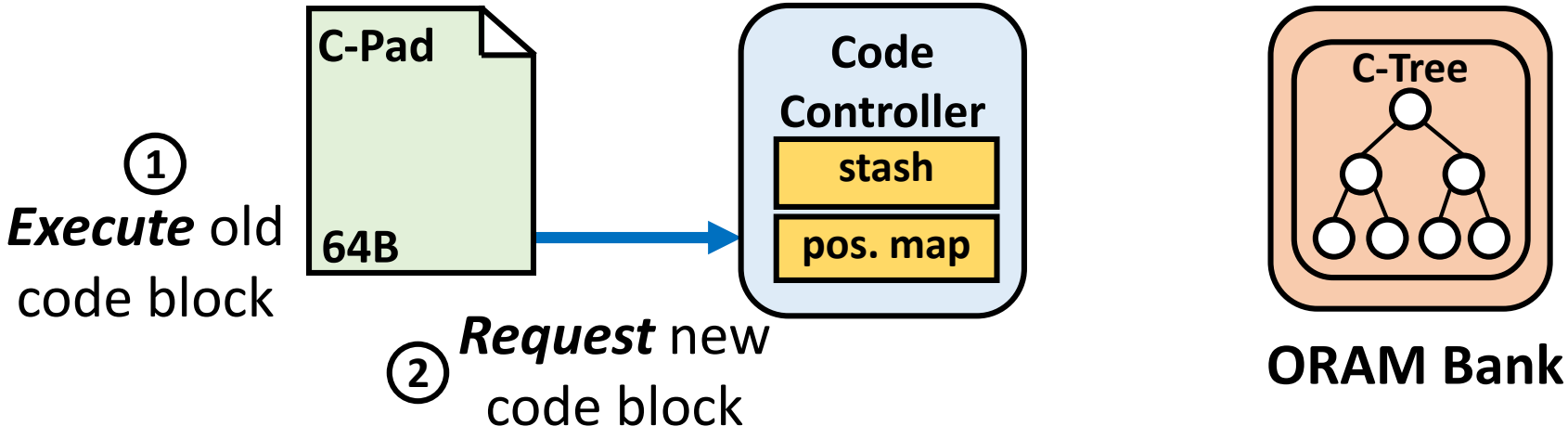

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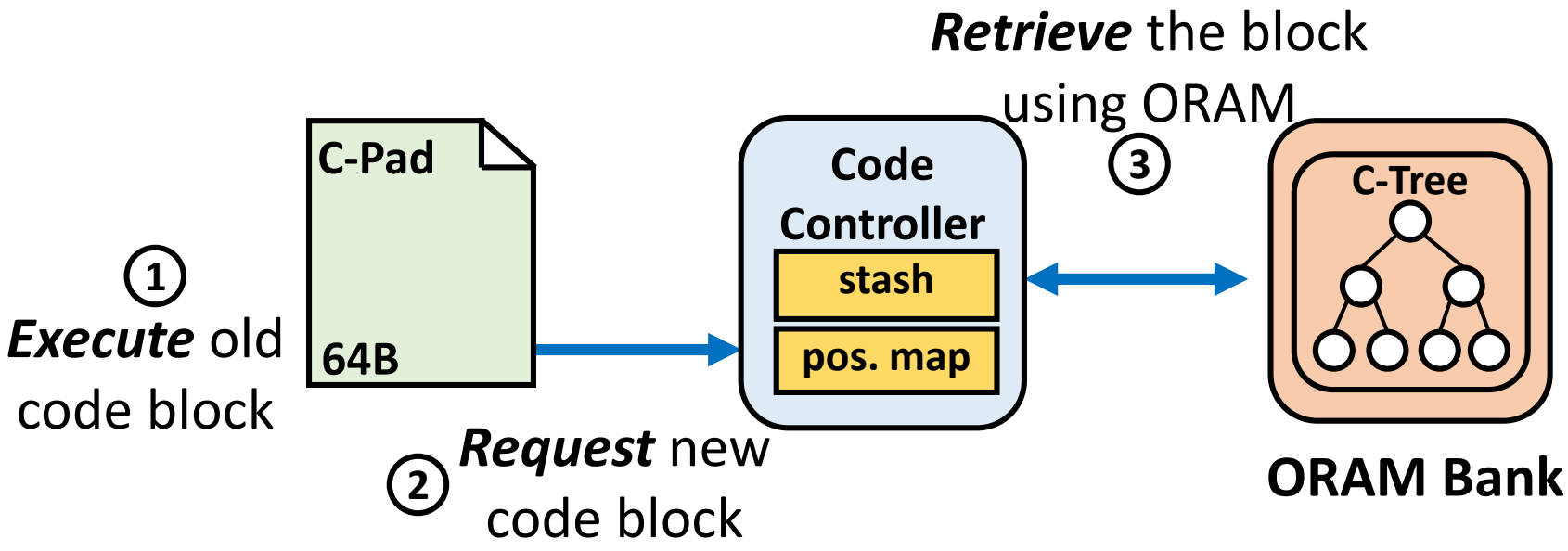

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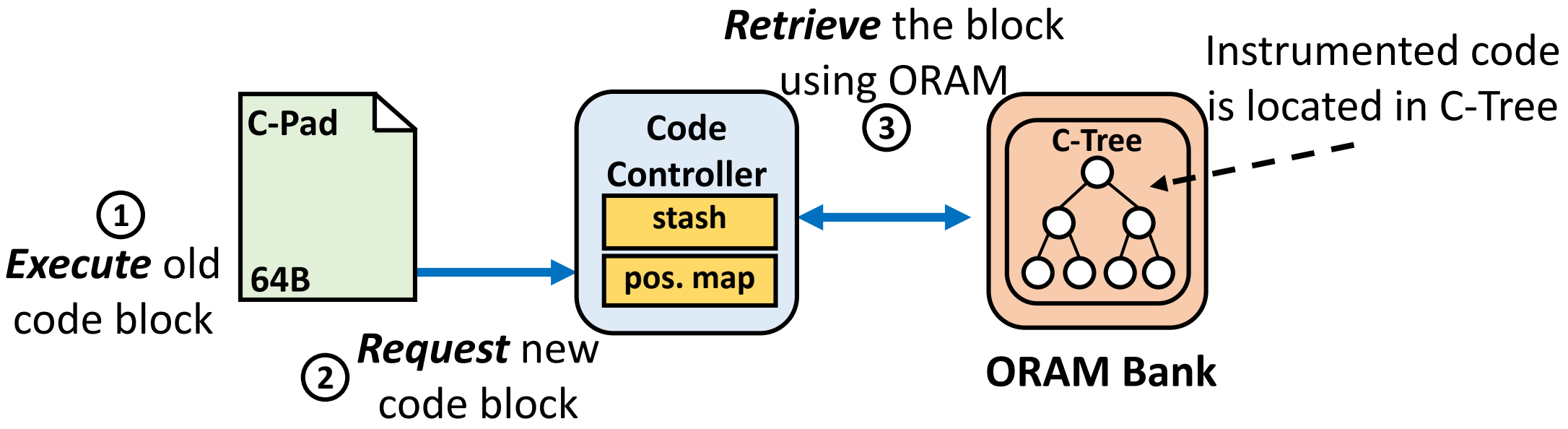

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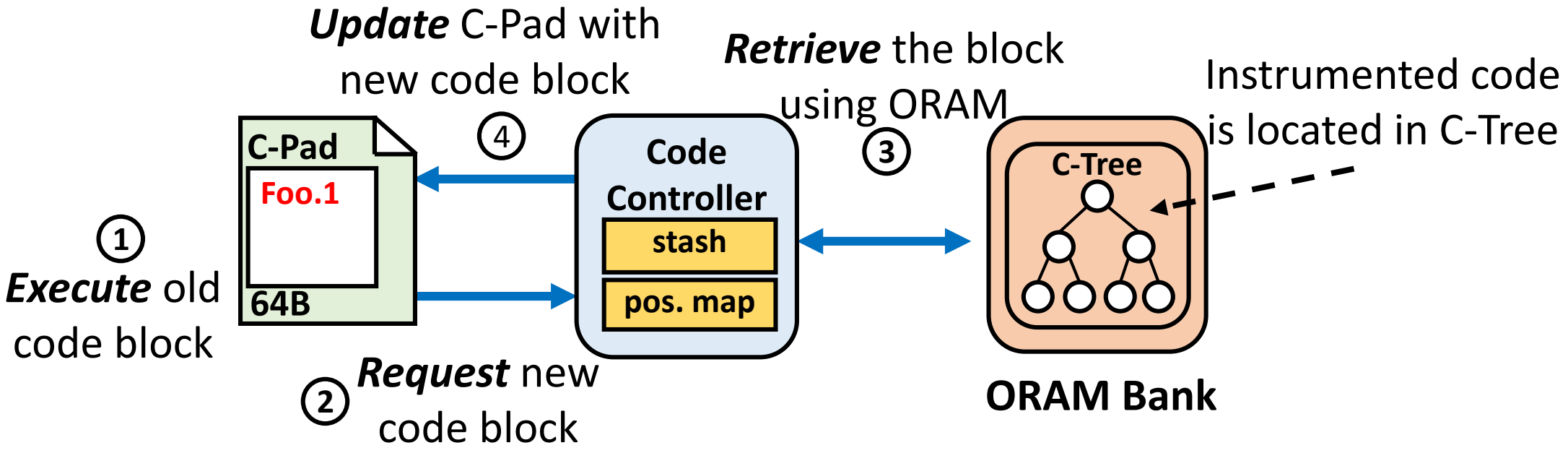

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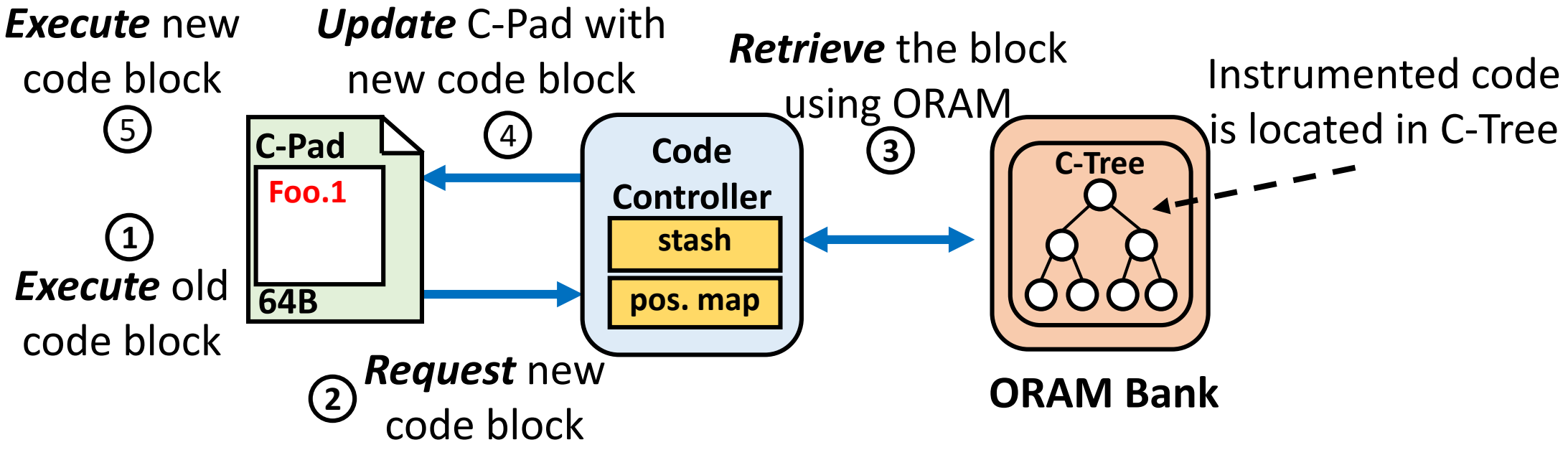

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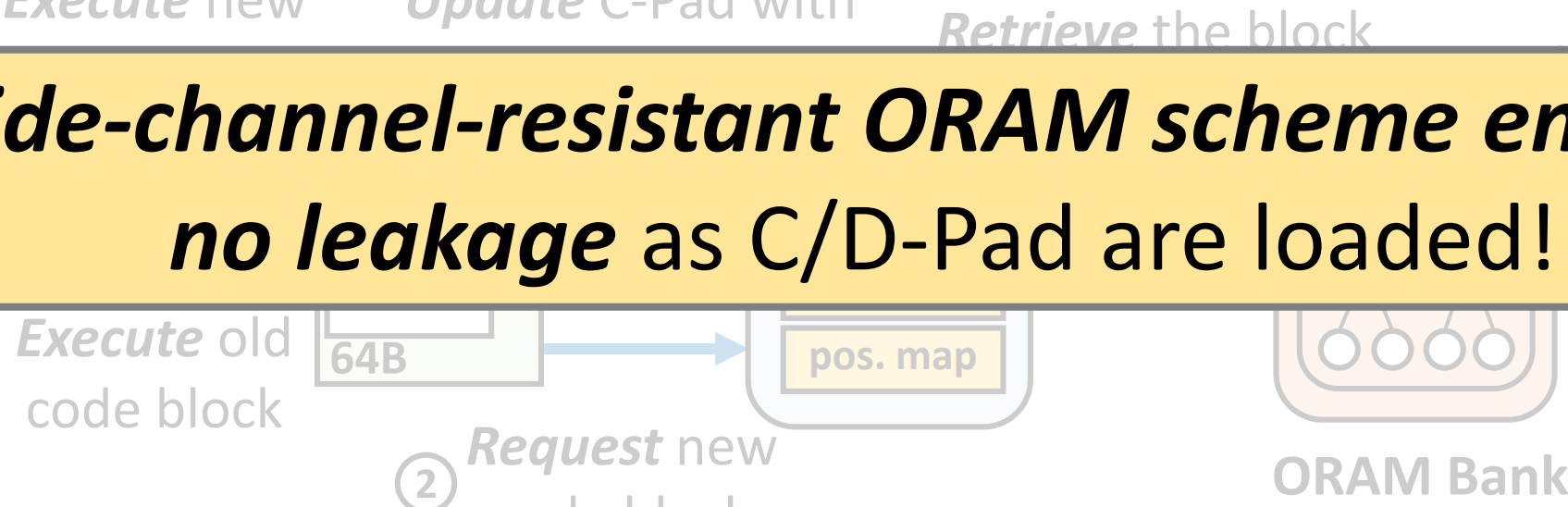

Side-channel-resistant ORAM scheme ensures no leakage as C/D-Pad are loaded!

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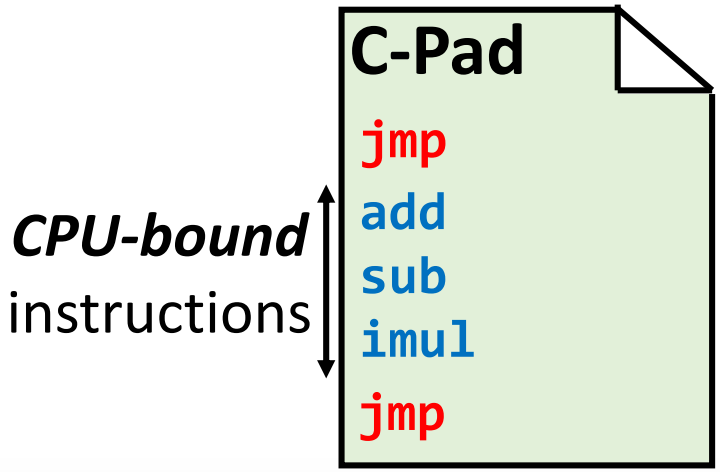

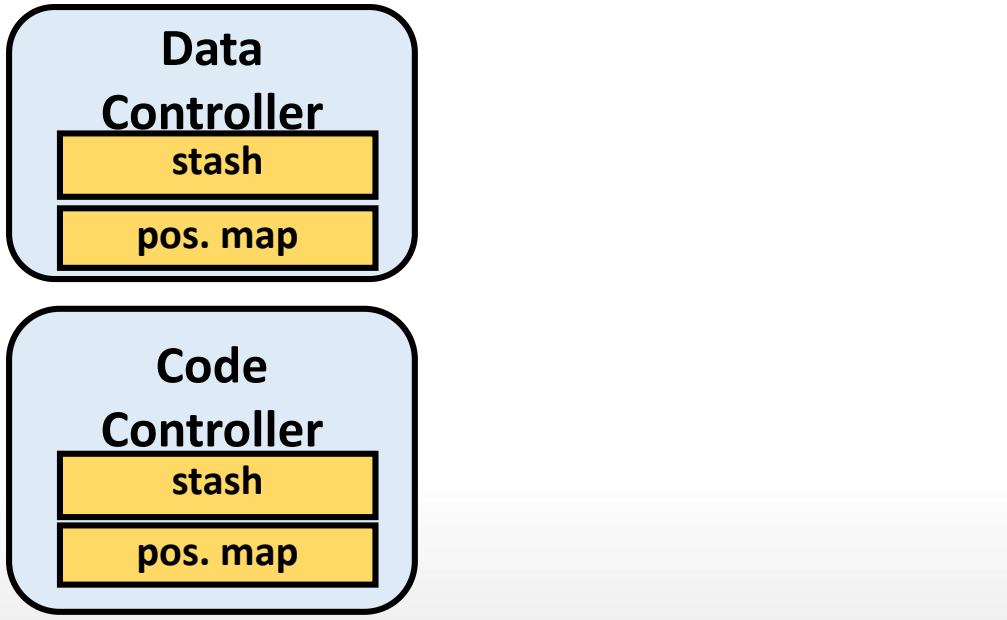

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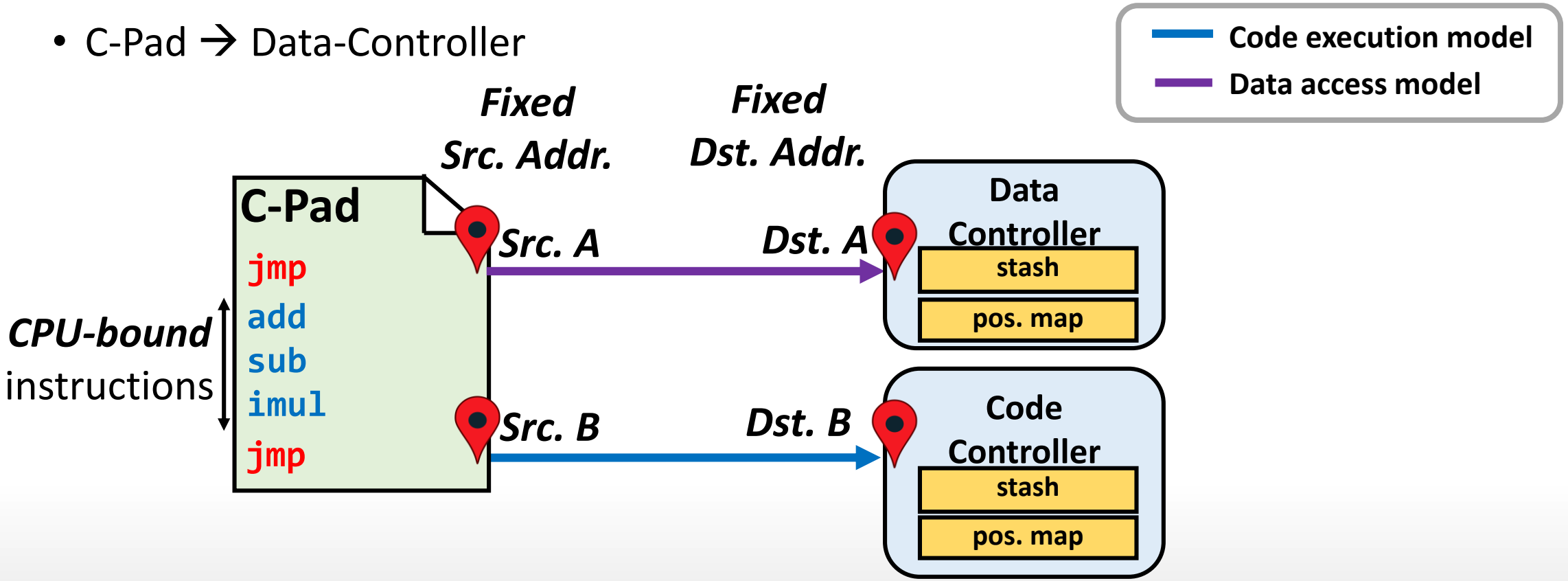

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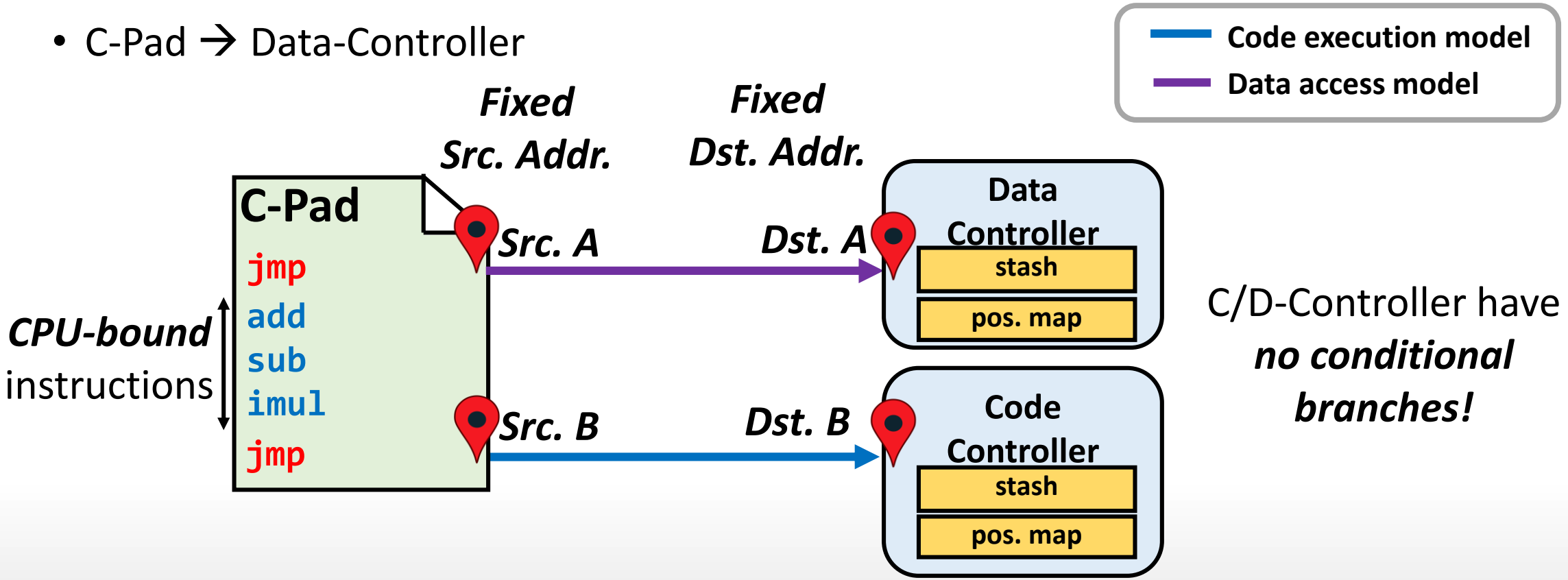

C/D-Controller have ***no conditional branches!***

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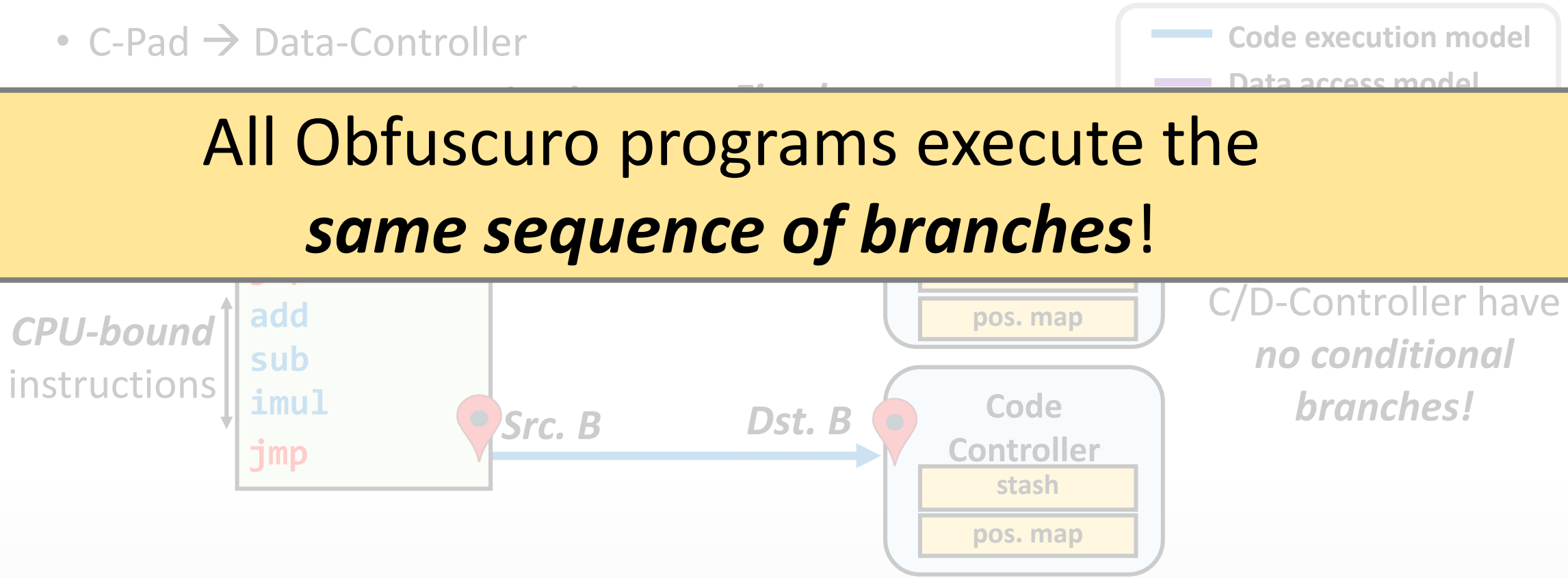
All Obfuscuro programs execute the ***same sequence of branches***!



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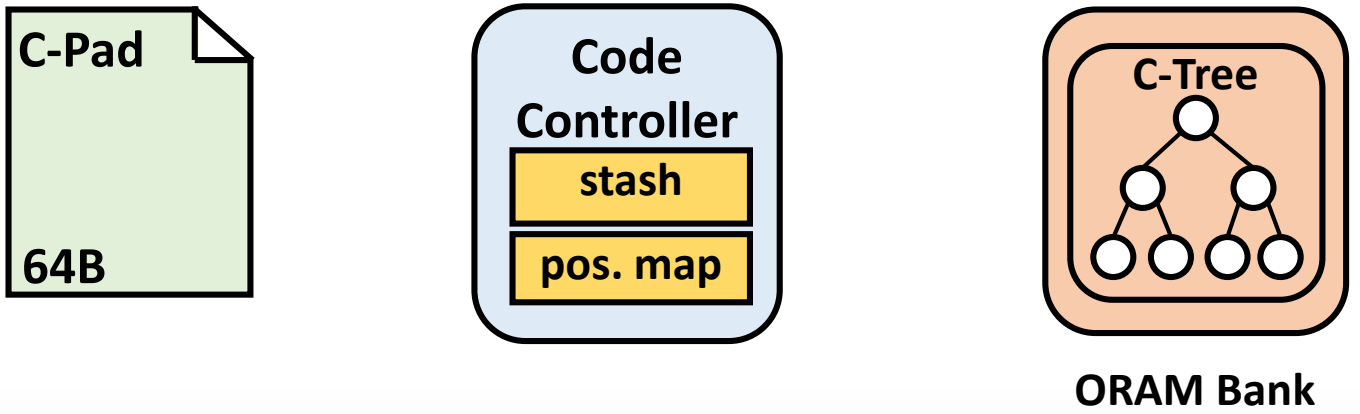

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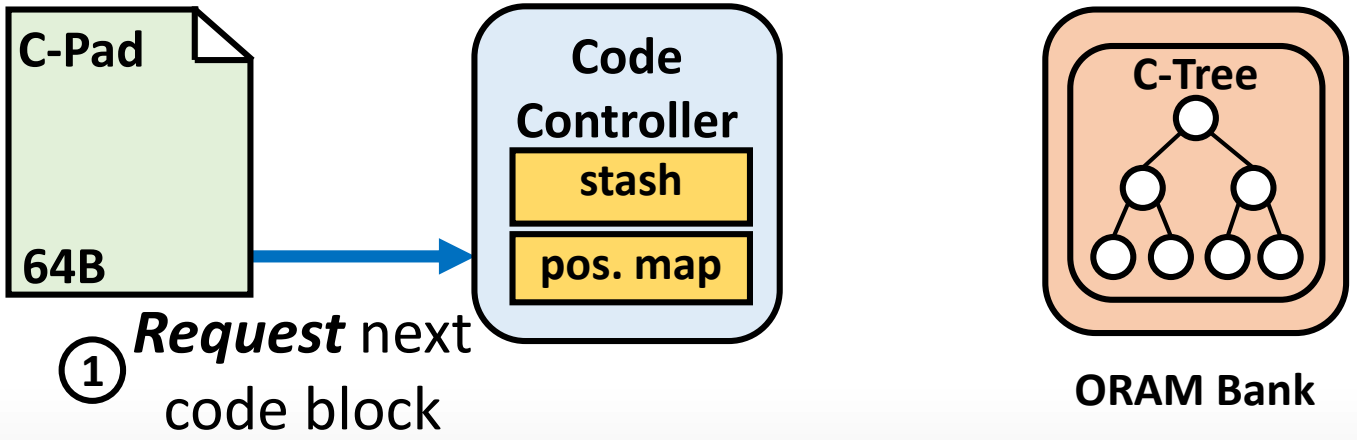

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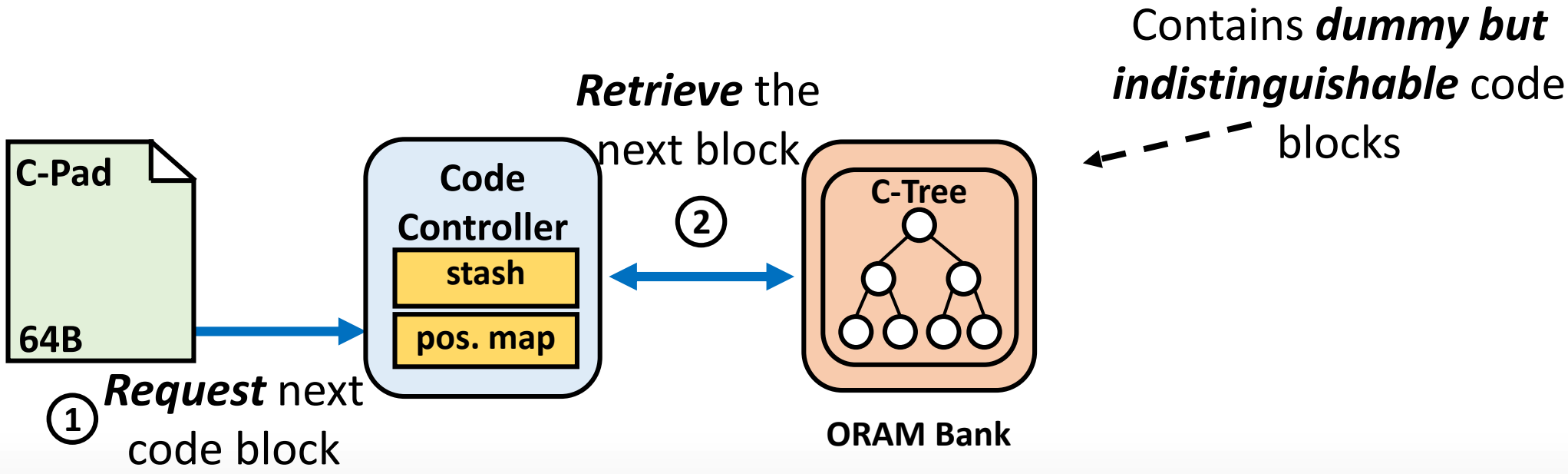

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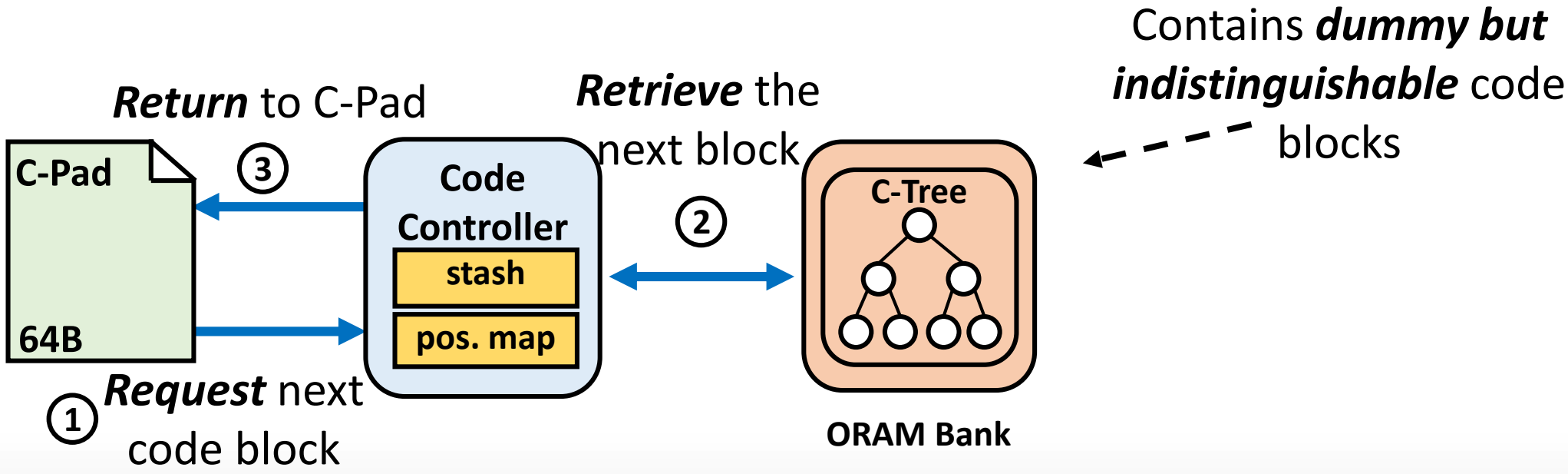

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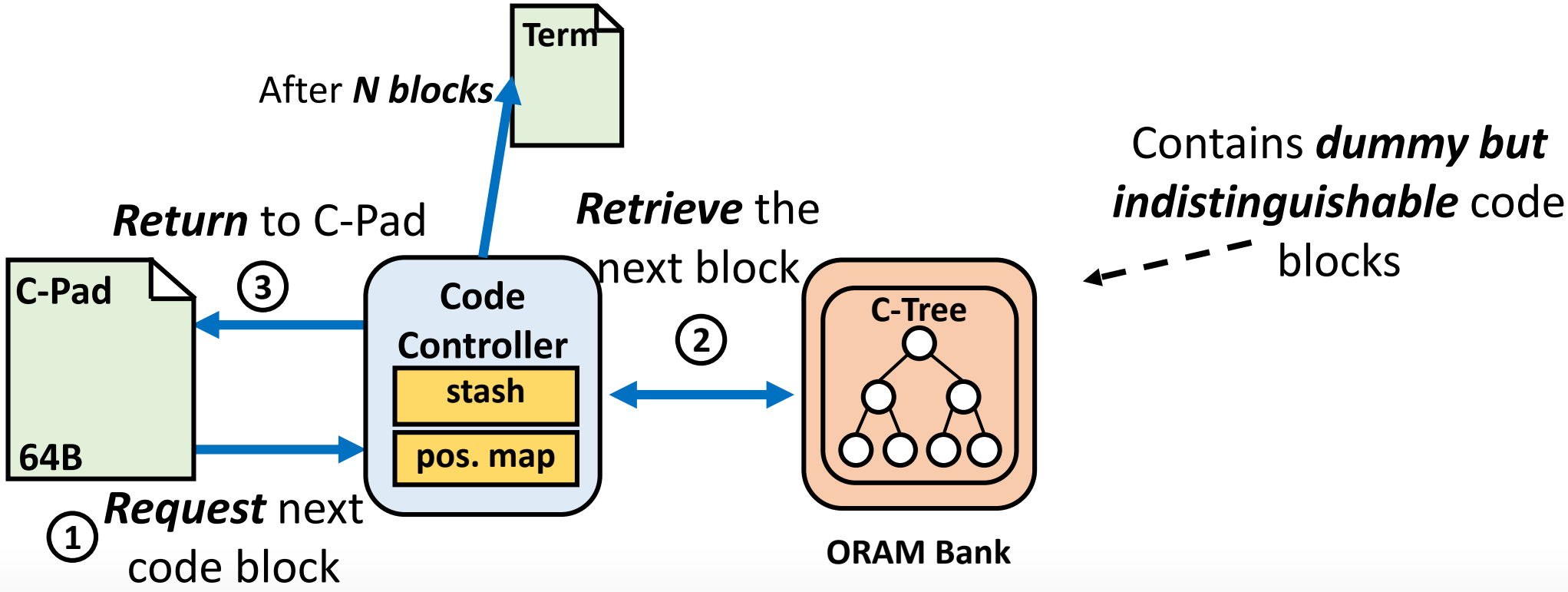

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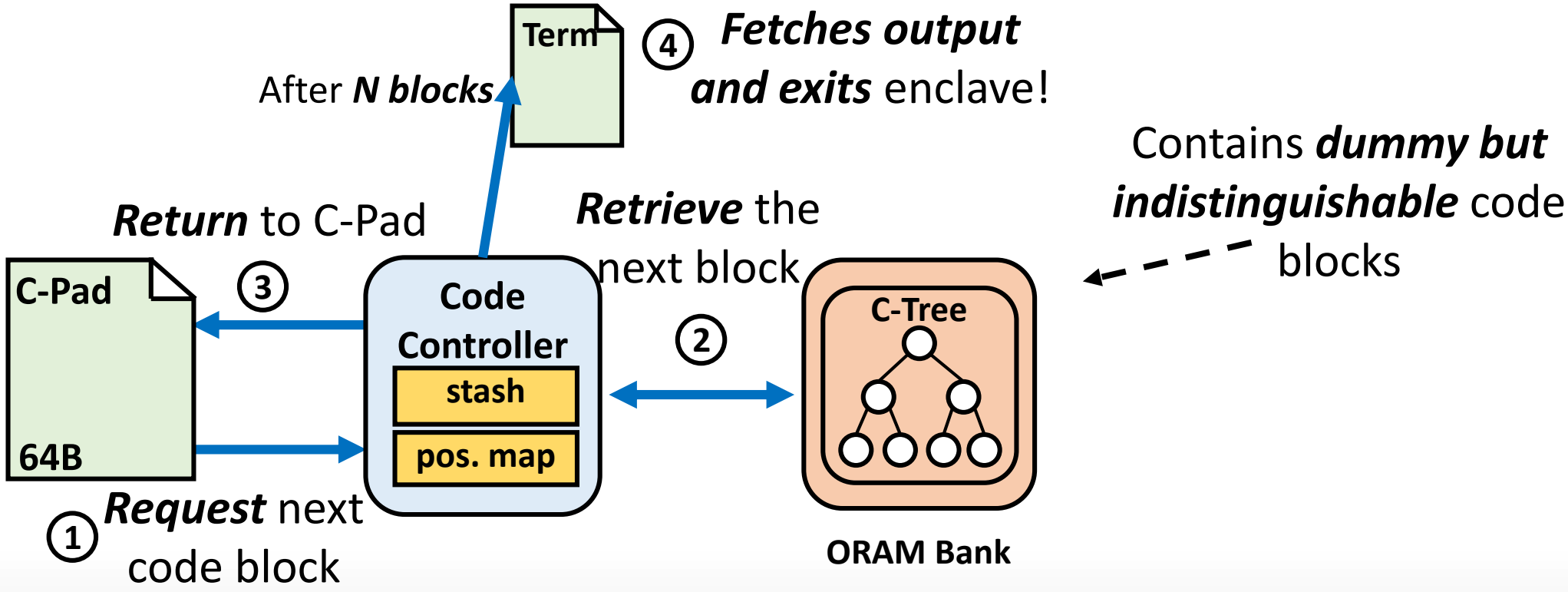

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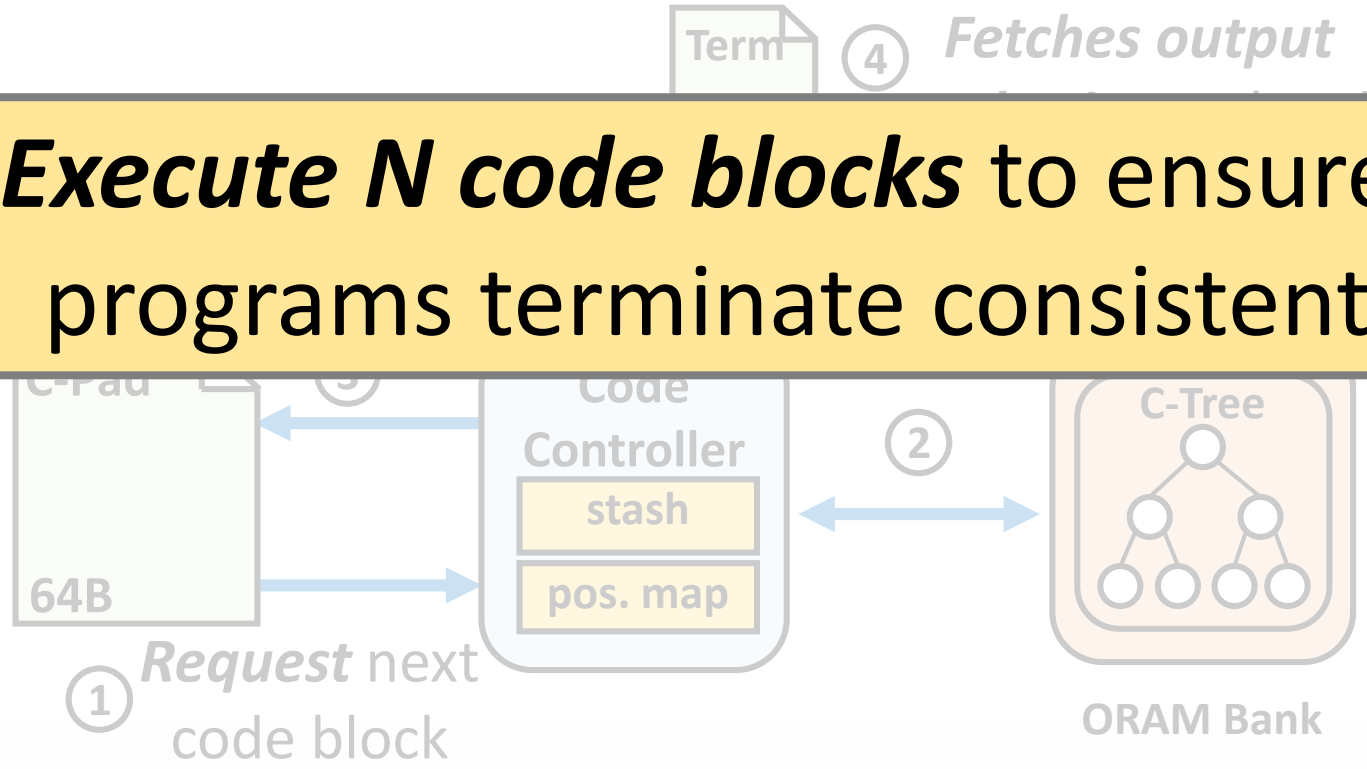

Execute N code blocks to ensure all programs terminate consistently!

Faster memory store for enclaves

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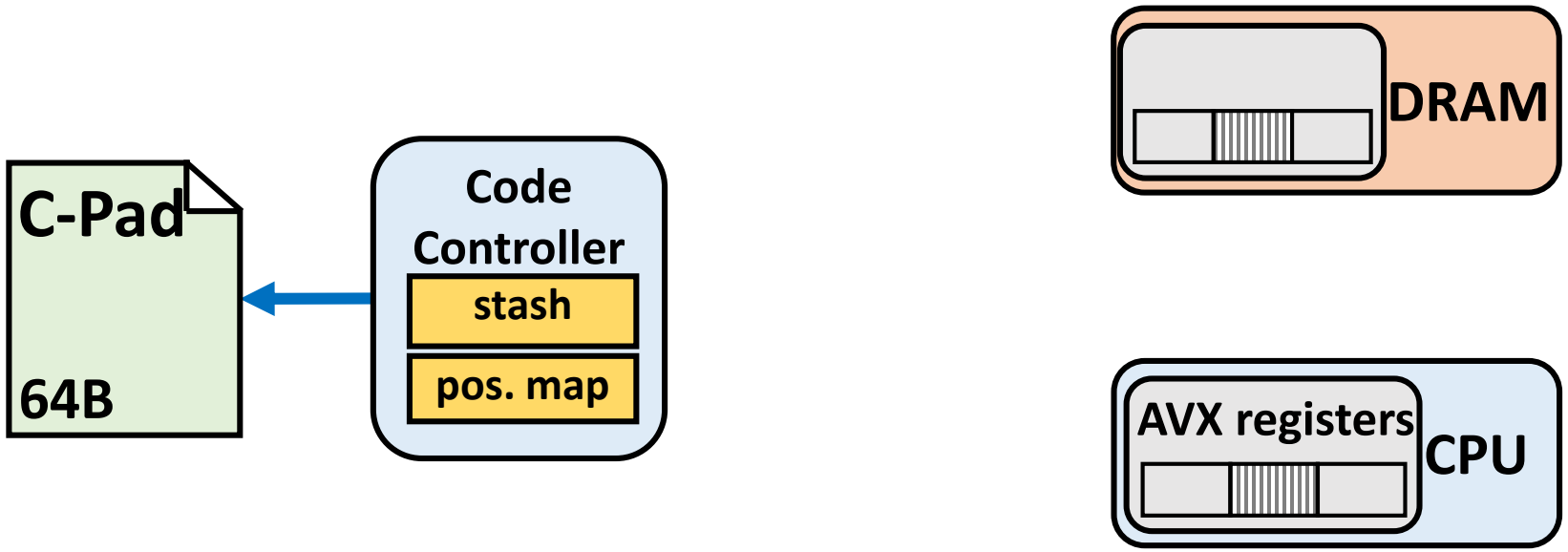

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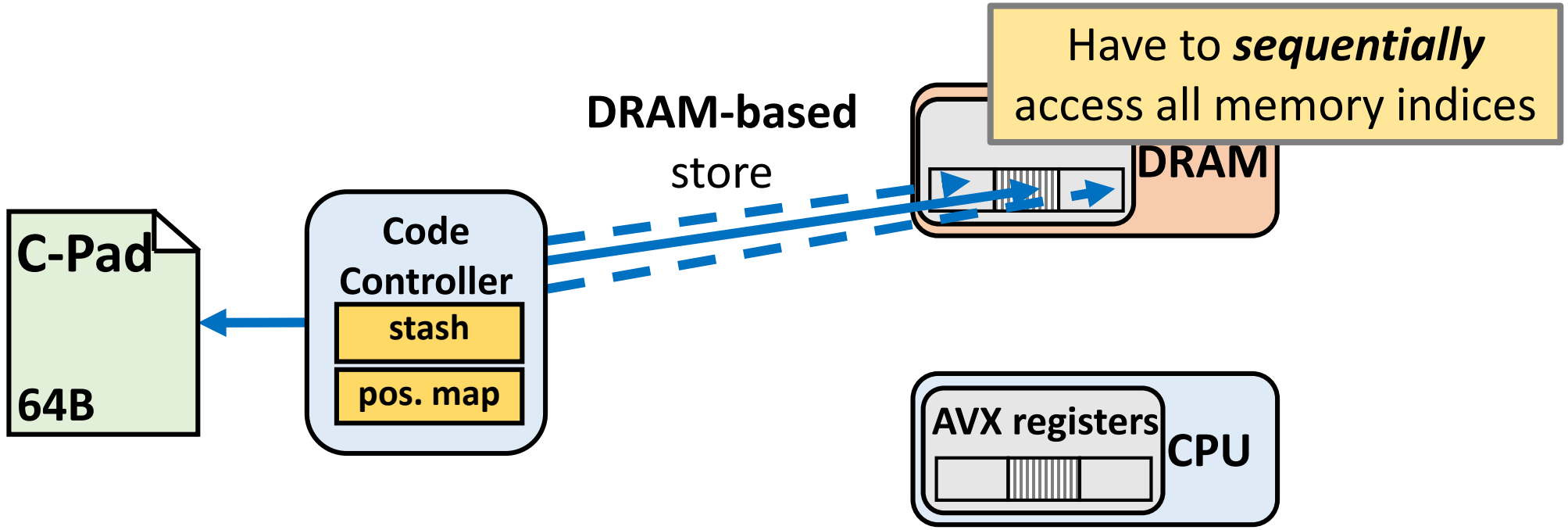

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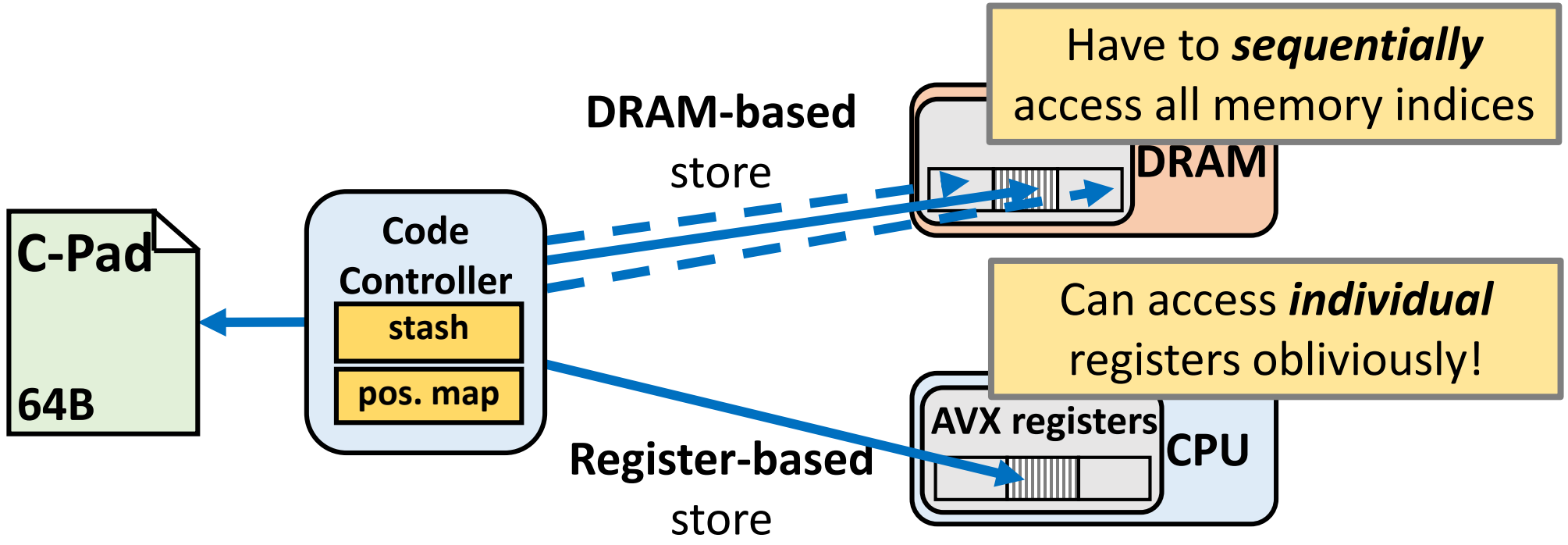

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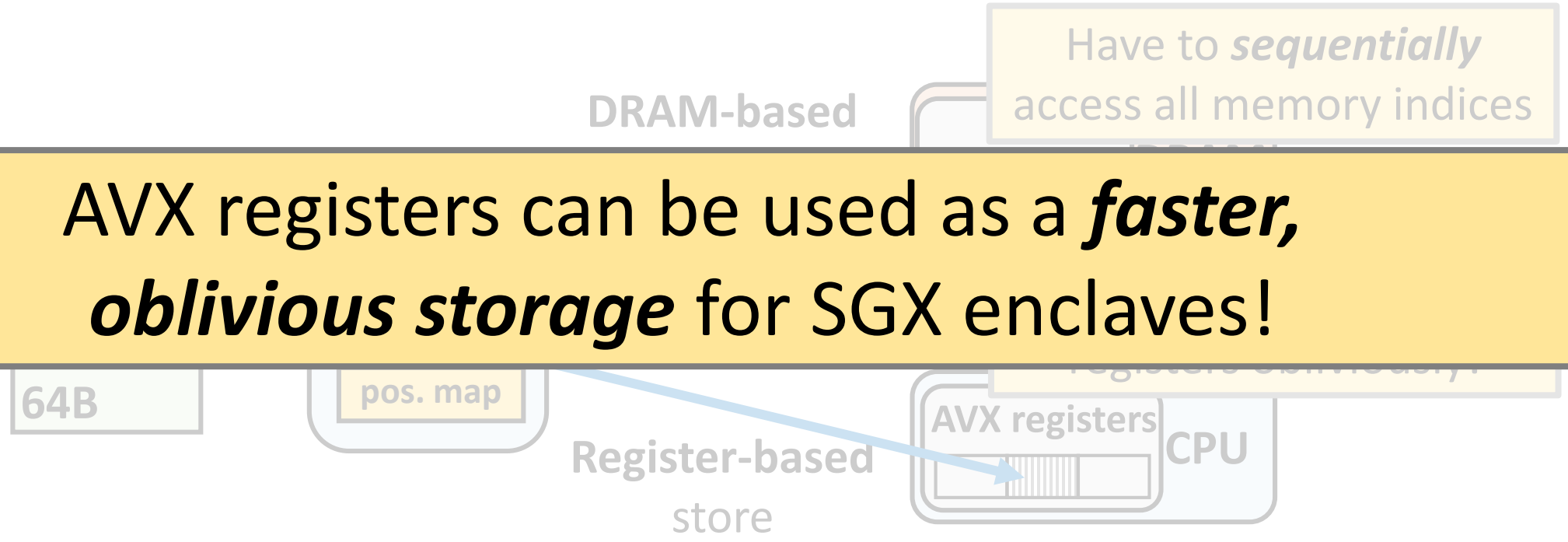

AVX registers can be used as a ***faster, oblivious storage*** for SGX enclaves!

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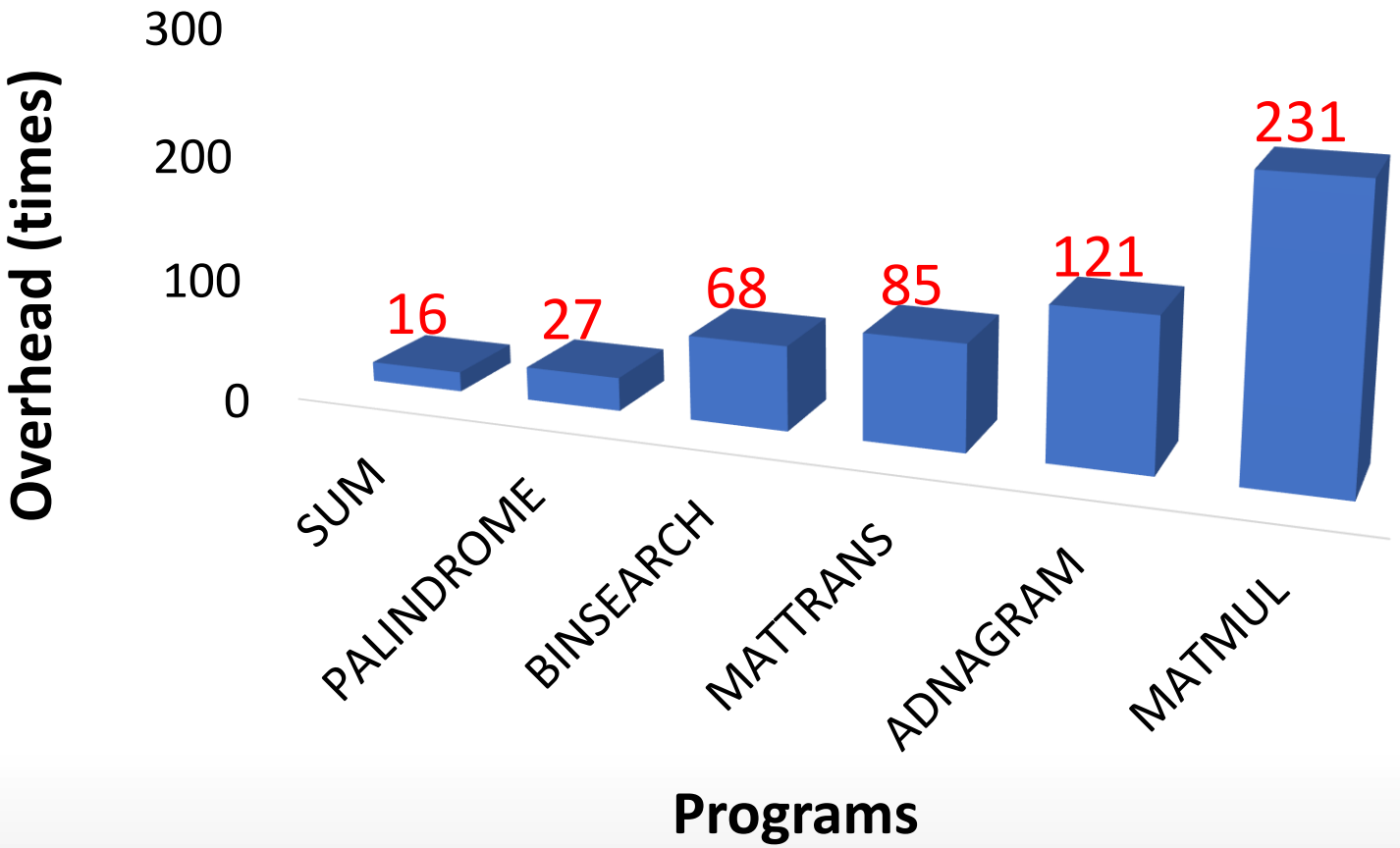
- **Intel SGX SDK (25 LoC)**
  - Assign memory regions for C/D-Pad **(support)**

Performance Evaluation



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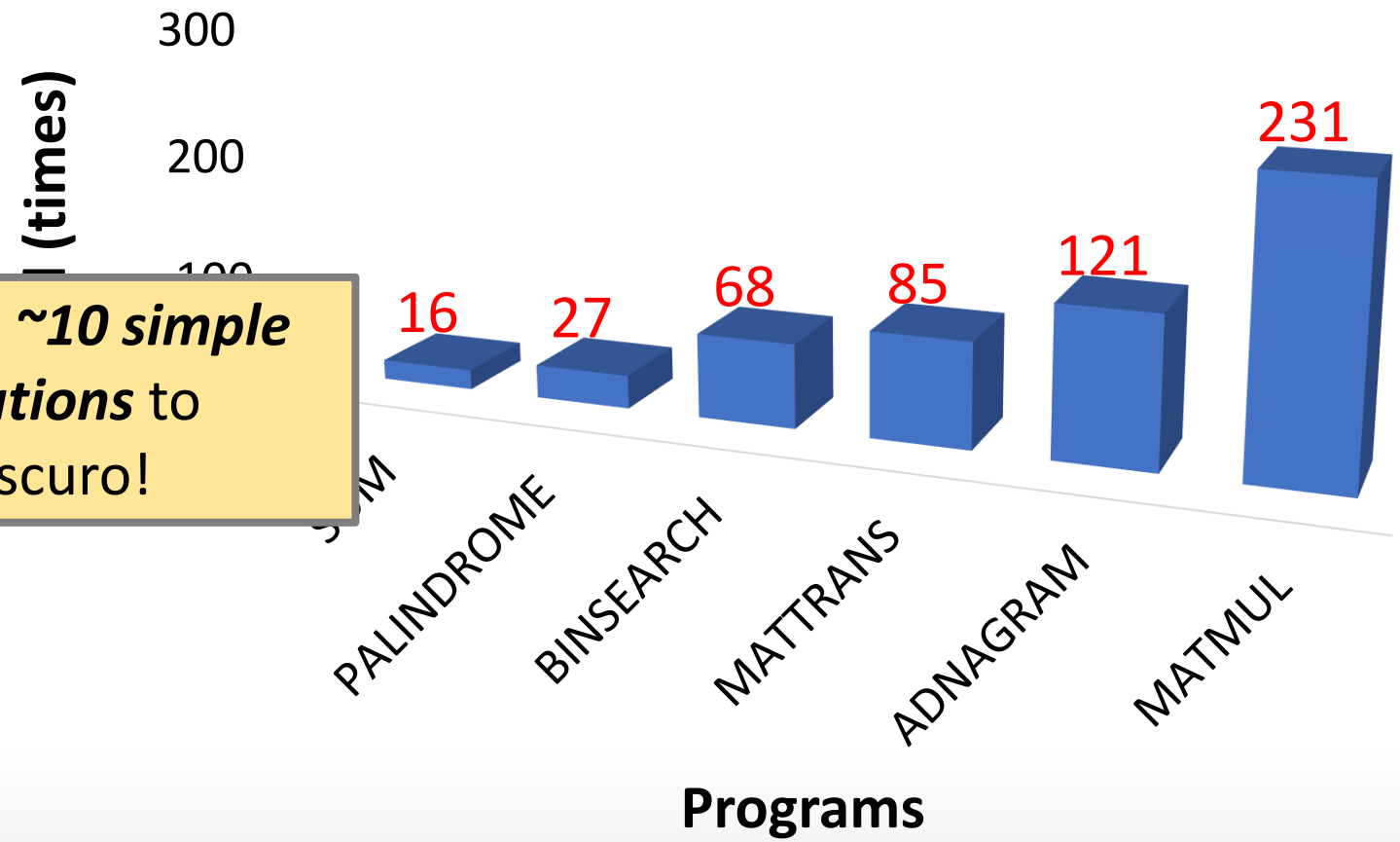

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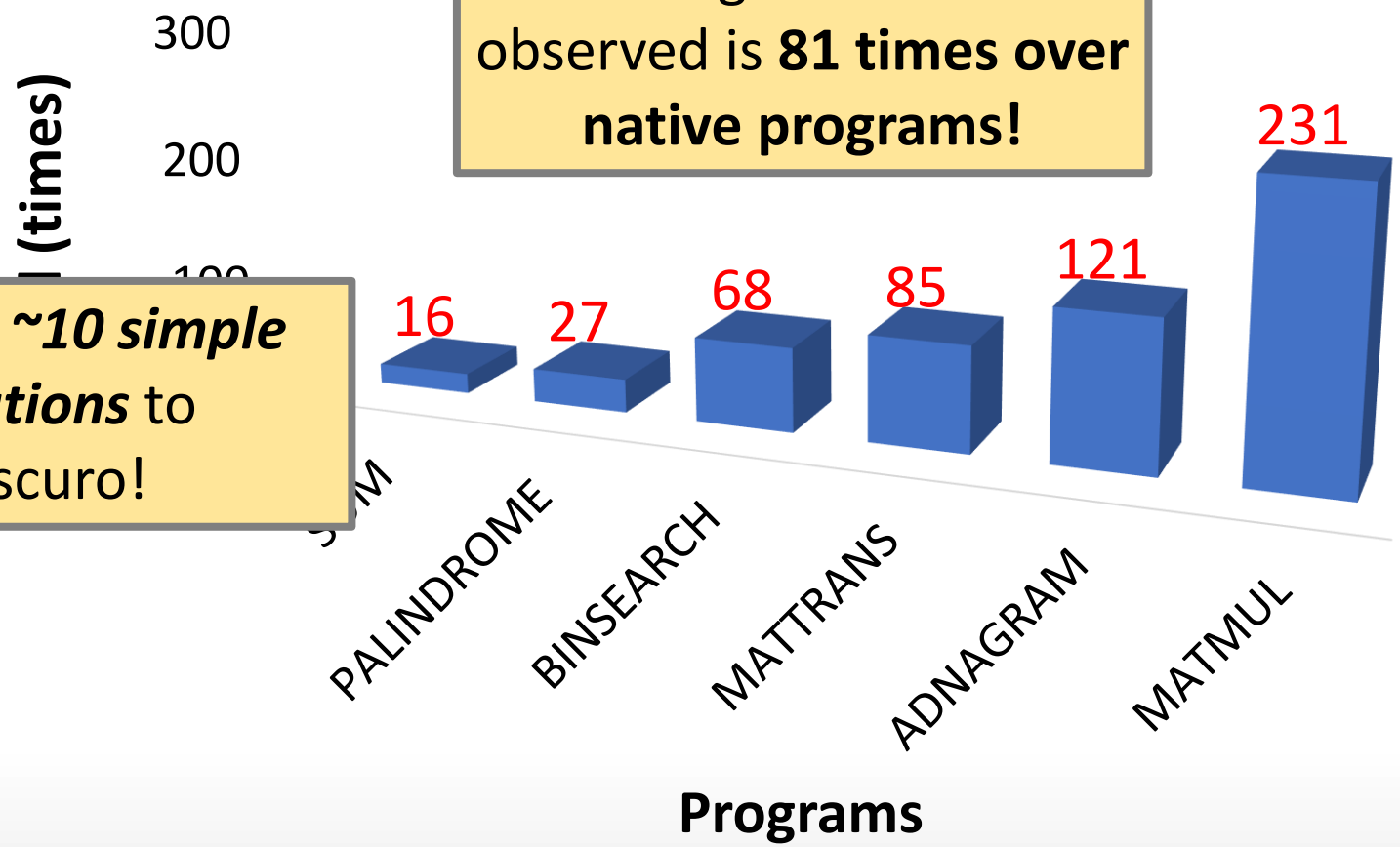

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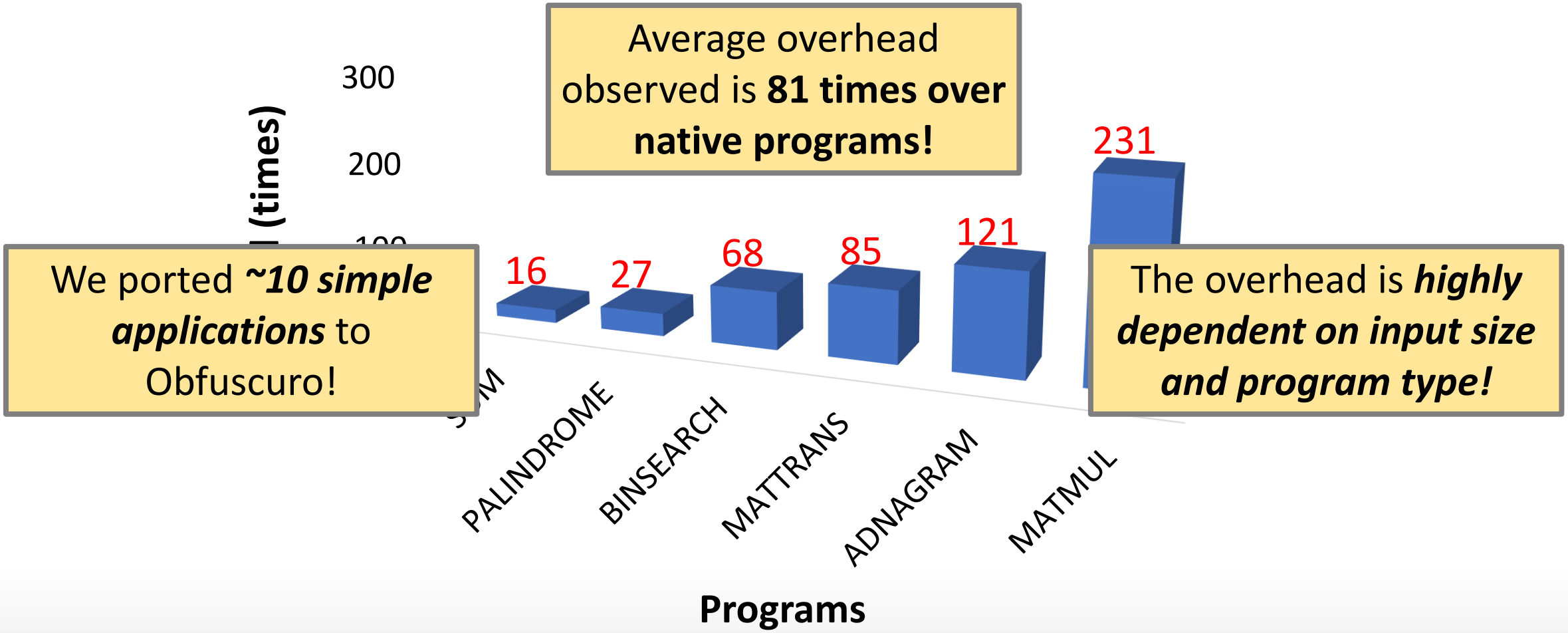

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The overhead is ***highly dependent on input size and program type!***

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3. Existing solutions have a ***limited approach*** towards side-channel mitigation in Intel SGX
4. Obfuscuro is compiler-based scheme which addresses this issue by ensuring all programs leak ***same access patterns***

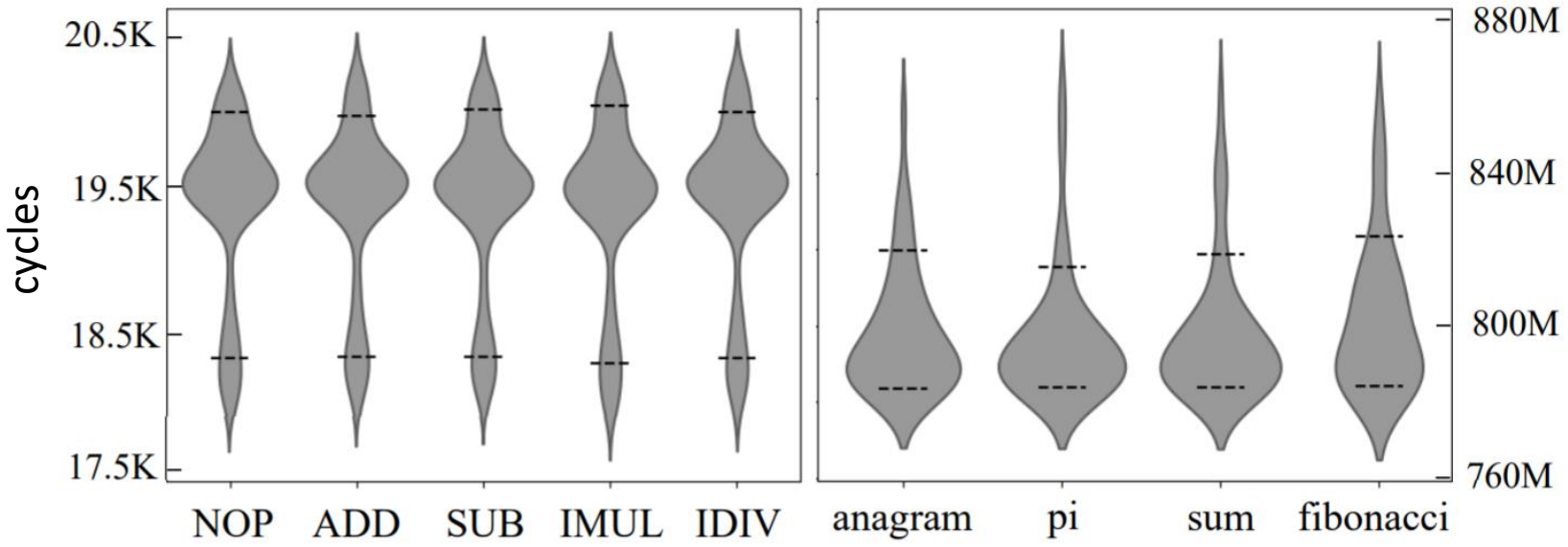
Adil Ahmad

Contact: ahmad37@purdue.edu

감사합니다

(Translation ~ **Thanks!**) ;)

Execution Time Evaluation



Code block with instructions of each type

General programs

ORAM access time dominates the time of code block execution!